Intel® X48 Express Chipset Memory Technology and Configuration Guide

White Paper

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Revision History

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-001	Initial release	March 2008

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1 Introduction

This document details the Intel® X48 Express Chipset system memory technology enhancements, supported memory configurations, and memory organizations. It is intended for a technical audience interested in learning about the performance enhancements and simplified population rules offered by Intel® Fast Memory Access and Intel® Flex Memory Technology in the platforms based on the Intel X48 Express Chipset.

2 Technology Enhancements of Intel® Fast Memory Access (Intel® FMA)

This chapter details Intel® X48 Express Chipset technology enhancements of its memory controller known as Intel® Fast Memory Access (Intel® FMA). The memory controller is located on the chipset's 82X48 Memory Controller Hub (MCH) component.

With the growing reliance on faster and less latent memory technologies for today's high performance platforms, it has become necessary to not only increase system memory transfer rate speeds, but to also streamline usage of the memory controller protocol in novel and intelligent ways to decrease latency and optimize memory bandwidth. To do this, several Intel technologies, known collectively as Intel® FMA, have been included in this generation of Intel's chipsets.

The following sections outline and explain the technology enhancements: Just In Time Scheduling, Command Overlap, Out of Order Scheduling, and Opportunistic Writes.

2.1 Just in Time Command Scheduling

The Intel X48 Express Chipset has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just In Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for the optimization of bandwidth and reducing of latency while retaining system memory protocol.

2.2 Command Overlap

Command Overlap allows for the insertion of the DRAM commands between the Activate, Precharge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. This allows for situations where multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

2.3 Out of Order Scheduling

Leveraging Just In Time Scheduling and Command Overlap, the Intel X48 Express Chipset continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the Intel X48 Express Chipset to further reduce latency and increase bandwidth efficiency. This is especially important for helping overcome the in-order manner of the Front Side Bus between the Intel X48 Express Chipset and the processor to minimize processor starvation.

2.4 Opportunistic Writes

Processor requests for memory reads usually are weighted more heavily than writes to memory to avoid cases of starving the processor of data to process while the writes are issued to system memory. Instead of having writes issued to a pending queue to be flushed to memory when certain watermarks are reached, which could starve the processor of data while it waits for the write flush to finish, the Intel X48 Express Chipset monitors system memory requests and issues pending write requests to memory at times when they will not impact memory read requests. This allows for an almost continuous flow of data to the processor for processing.

3 Supported Memory Technologies and Configurations

3.1 Memory Technology Supported

The X48 Express Chipset supports the following DDR3 Data Transfer Rates, DIMM Modules, and DRAM Device Technologies:

- DDR3 Data Transfer Rates:
  - 800 (PC3-6400), 1067 (PC3-8500), 1333 (PC3-10600), and 1600 (PC3-12800)
    - 1600 memory support requires approved Intel Extreme Memory Profile (XMP) 1600 DIMMs.
- DDR3 DIMM Modules:
  - Raw Card A - Single Sided x8 un-buffered non-ECC
  - Raw Card B - Double Sided x8 un-buffered non-ECC
  - Raw Card C - Single Sided x16 un-buffered non-ECC
  - For DDR3 1600 transfer rates the X48 Express Chipset only supports approved Raw Card A single sided x8 un-buffered non-ECC Intel XMP-1600 DIMM modules.
- DDR3 DRAM Device Technology:
  - 512 Mb and 1 Gb

Table 3-1. Memory Technology Support Details

Mem. Type	Raw Card Ver.	DIMM Cap.	DRAM Device Tech.	DRAM Org.	# of DRAM Devices	# of Physical Device Ranks	# of Row /Col Address Bits	# of Banks Inside DRAM	Page Size	Notes
DDR3 800, 1067, 1333	A	512 MB	512 MB	64M X 8	8	1	13/10	8	8K	
		1 GB	1 GB	128M X 8	8	1	14/10	8	8K	
	B	1 GB	512 MB	64M X 8	16	2	13/10	8	8K	
		2 GB	1 GB	128M X 8	16	2	14/10	8	8K	
	C	256 MB	512 MB	32M X 16	4	1	12/10	8	8K	
		512 MB	1 GB	64M X 16	4	1	13/10	8	8K	
DDR3 1600	A	512 MB	512 MB	64M X 8	8	1	13/10	8	8K	1
		1 GB	1 GB	128M X 8	8	1	14/10	8	8K	

NOTES:

1. For DDR3 1600 transfer rates the X48 Express Chipset only supports approved Raw Card A single sided x8 un-buffered non-ECC Intel® XMP DDR3-1600 DIMM modules.

3.2 DRAM Device Timing Support

The X48 Express Chipset supports the following DDR3 DRAM Device Speed Bin and Write Latency (WL) Timings on the main memory interface.

Table 3-2. DDR3 DRAM Device Timing Support

Memory Type	DRAM Data Rate	t_{CL}	t_{RCD}	t_{RP}	WL	Units
DDR3	800 MT/s	5	5	5	5	tCK
		6	6	6	5	tCK
	1067 MT/s	7	7	7	6	tCK
		8	8	8	6	tCK
	1333 MT/s	8	8	8	7	tCK
		9	9	9	7	tCK
		10	10	10	7	tCK
	1600 MT/s	8	8	8	8	tCK
		9	9	9	8	tCK
		10	10	10	8	tCK
		11	11	11	8	tCK

3.3 ECC Support

For DDR3 the X48 Express Chipset does **NOT** support ECC, does not support ECC un-buffered DIMMs, and it does not support any memory configuration that mixes non-ECC with ECC un-buffered DIMMs.

See Section 3.1 for un-buffered DIMM support details.

3.4 Intel® Extreme Memory Profile (XMP) Support

The Intel Extreme Memory Profile (XMP) provides a simple and robust high performance 1600 memory solution for Intel based platforms using the X48 Express Chipset. Intel co-developed the Extreme Memory Profile (XMP) specification with its memory partners to enable performance tuning of DDR3 memory to beyond standard JEDEC SPD specifications. This benefits the user by enabling both the novice (using built-in profiles) and the advanced users (by allowing manual timing parameter adjustments) to tune the performance of their Intel platforms.

This profile based solution enables the X48 Extreme Chipset to support 1600 allowing new extreme levels of memory performance.

3.5 Valid Front Side Bus and Memory Speeds

The X48 Express Chipset supports the following Front Side Bus (FSB) and system memory speed configurations.

Table 3-3. Intel® X48 Valid FSB/Memory Speed Configurations

Memory Type	FSB	DRAM Data Rate	Single Channel Peak Bandwidth	Dual Channel Peak Bandwidth
DDR3	1600 MHz	1600 MT/s	12.8GB/s	25.6 GB/s
	1600 MHz	1067 MT/s	8.5 GB/s	17.0 GB/s
	1333 MHz	1333 MT/s	10.5 GB/s	21.0 GB/s
	1333 MHz	1067 MT/s	8.5 GB/s	17.0 GB/s
	1333 MHz	800 MT/s	6.4 GB/s	12.8 GB/s
	1067 MHz	1067 MT/s	8.5 GB/s	17.0 GB/s
	1067 MHz	800 MT/s	6.4 GB/s	12.8 GB/s
	800 MHz	800 MT/s	6.4 GB/s	12.8 GB/s

Note: The X48 Express Chipset does not support system memory frequencies that exceed the frequency of the Front Side Bus. If memory with higher frequency capabilities than that of the FSB is populated, the memory will be under-clocked to align with the FSB.

3.6 System Memory DIMM Configuration Support

The X48 Express Chipset directly supports one or two channels of DDR3 memory with the following DDR3 DIMM configurations:

— Supports one or two DDR3 DIMM modules per channel at DDR3 800, 1067, and 1333 data transfer rates.

— Supports only one DDR3-DIMM module per channel where DIMM1 (furthest) is populated and DIMM0 (closet) is not populated at DDR3-1600 data transfer rates.

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4 Memory Organization and Operating Modes

The Intel X48 Express Chipset memory interface is designed with Intel® Flex Memory Technology, so that it can be can be configured to support single-channel or dual-channel DDR3 memory configurations. Depending upon how the DIMMs are populated in each memory channel, a number of different configurations can exist for DDR3.

The following sections explain and show the different memory configurations that are supported by the X48 Express Chipset.

4.1 Single-Channel Mode

In this mode, all memory cycles are directed to a single channel.

Single channel mode is used when either Channel-0 or Channel-1 DIMMs are populated in any order, but not both.

4.2 Dual Channel Modes

4.2.1 Dual Channel Symmetric Mode

This mode provides maximum performance on real applications. Addresses are ping-ponged between the channels after each cache line (64 byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels.

Dual channel symmetric mode is used when both Channel-0 and Channel-1 DIMMs are populated in any order with the total amount of memory in each channel being the same, but the DRAM device technology and width may vary from one channel to the other.

Table 4-1 is a sample dual channel symmetric memory configuration showing the rank organization.

Table 4-1. Sample Dual Channel Symmetric Organization Mode

Rank	Channel 0 Population	Cumulative Top Address in Channel 0	Channel 1 Population	Cumulative Top Address in Channel 1
Rank 3	0 MB	2560 MB	0 MB	2560 MB
Rank 2	256 MB	2560 MB	256 MB	2560 MB
Rank 1	512 MB	2048 MB	512 MB	2048 MB
Rank 0	512 MB	1024 MB	512 MB	1024 MB

4.2.2 Dual Channel Asymmetric Modes

4.2.2.1 Stacked Asymmetric Mode

In this addressing mode addresses start in channel-0 and stay there until the end of the highest rank in channel-0, and then addresses continue from the bottom of channel-1 to the top.

This mode is used when both Channel-0 and Channel-1 DIMMs are populated in any order with the total amount of memory in each channel being different.

Table 4-2 is a sample dual channel stacked asymmetric memory configuration showing the rank organization.

Table 4-2. Sample Dual Channel Stacked Asymmetric Organization Mode

Rank	Channel 0 Population	Cumulative Top Address in Channel 0	Channel 1 Population	Cumulative Top Address in Channel 1
Rank 3	0 MB	1280 MB	0 MB	2304 MB
Rank 2	256 MB	1280 MB	0 MB	2304 MB
Rank 1	512 MB	1024 MB	512 MB	2304 MB
Rank 0	512 MB	512 MB	512 MB	1792 MB

4.2.2.2 L-shaped Asymmetric Mode

In this addressing mode the lowest DRAM memory is mapped to dual channel operation and the top most DRAM memory is mapped to single channel operation. In this mode the system can run at one zone of dual channel mode and one zone of single channel mode simultaneously across the whole memory array.

This mode is used when both Channel-0 and Channel-1 DIMMs are populated in any order with the total amount of memory in each channel being different.

Table 4-3 is a sample dual channel L-shaped asymmetric memory configuration showing the rank organization.

Table 4-3. Sample Dual Channel L-Shaped Asymmetric Organization Mode

Rank	Channel 0 Population	Cumulative Top Address in Channel 0	Channel 1 Population	Cumulative Top Address in Channel 1
Rank 3	0 MB	2048 MB	0 MB	2304 MB
Rank 2	0 MB	2048 MB	256 MB	2304 MB
Rank 1	512 MB	2048 MB	512 MB	2048 MB
Rank 0	512 MB	1024 MB	512 MB	1024 MB

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