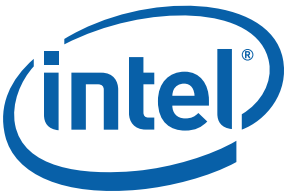

# Intel® X38 Express Chipset

## Specification Update

### — For the 82X38 Memory Controller Hub (MCH)

**February 2008**

Document Number: 317611-003

# Contents

# 1 Revision History

| Revision | Description | Date |
|---|---|---|
| -001 | • Initial release. | November 2007 |
| -002 | • Added Erratum 3.<br>• Added Document Changes 1 and 2. | December 2007 |
| -003 | • Added Documentation Change #3 | February 2008 |

# 2 Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

## 2.1 Affected Documents

| Document Title | Document Number/Location |
|---|---|
| Intel® X38 Express Chipset Datasheet | 317610-001 |

## 2.2 Nomenclature

**Errata** are design defects or errors. These may cause the MCH's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

***Note:*** Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

# 3 Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the MCH product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

## 3.1 Codes Used in Summary Tables

### 3.1.1 Stepping

| | |
|---|---|
| X: | Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping. |
| (No mark) or (Blank box): | This erratum is fixed in listed stepping or specification change does not apply to listed stepping. |

### 3.1.2 Page

| | |
|---|---|
| (Page): | Page location of item in this document. |

### 3.1.3 Status

| | |
|---|---|
| Doc: | Document change or update will be implemented. |
| Plan Fix: | This erratum may be fixed in a future stepping of the product. |
| Fixed: | This erratum has been previously fixed. |
| No Fix: | There are no plans to fix this erratum. |

### 3.1.4 Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

## 3.2 Errata

| Number | Steppings | | Status | ERRATA |
|---|---|---|---|---|
| | A0 | A1 | | |
| 1 | X | X | No Fix | PCIe 1.1 cards in PCIe slots off the MCH lead to boot failures. |
| 2 | X | X | No Fix | Intermittent IERR# hangs during cold boot does not detect PCIe cards |
| 3 | X | X | No Fix | IERR due to DMI/PCIe Link Not Trained |

## 3.3 Specification Changes

| No. | SPECIFICATION CHANGES |
|---|---|
| - | There are no Specification Changes in this Specification Update revision. |

## 3.4 Specification Clarifications

| No. | SPECIFICATION CLARIFICATIONS |
|---|---|
| - | There are no Specification Changes in this Specification Update revision. |

## 3.5 Documentation Changes

| No. | DOCUMENTATION CHANGES |
|---|---|
| 1 | Error Checking and Correction |
| 2 | DDR3 ECC support |
| 3 | DDR3 (ECC) XOR Chains |

# 4 Identification Information

## 4.1 Component Marking Information

The Intel 82X38 MCH stepping can be identified by the following component markings.

| Stepping | Top Marking | Notes |
|---|---|---|
| A1 | NU82X38 SLALJ | Intel® X38 Express Chipset MCH - Production |

# 5 Errata

## 1. PCIe 1.1 cards in PCIe slots off the MCH lead to boot failures.

Problem: The Intel® X38 Express Chipset sets the TS1 Ordered Set - Symbol 4 Bit[6] to 1b when a PCIe 1.1 card is plugged in. This is a reserved bit which is used in PCIe 2.0 to broadcast support for selectable de-emphasis. PCIe 1.1 Specification states that Bit[6] should be set to 0b. With some 2.5 GT/s PCIe 1.1 I/O cards of widths x8/x4/x1, system restarts and hangs were exhibited during PCIe link initialization when populated in MCH slots.

Implication: System unable to train some 2.5 GT/s PCIe 1.1 cards that don't comply with the PCIe 1.1 Specification. Failures have occurred across multiple vendors and different types of PCIe 1.1 cards.

Workaround: Contact your Intel field representative for the latest BIOS information. Modification to the Link Stability/Recovery Algorithm will fix this issue when using non-compliant cards but customers should continue working with their card vendors for PCIe 1.1 Spec compliancy.

Status: No Fix. For affected steppings, see the Summary Table of Changes.

## 2. Intermittent IERR# hangs during cold boot does not detect PCIe cards.

Problem: During cold boots, the MCH may hang during power-on and assert IERR or may not detect PCIe cards off the primary port or secondary port. The 1.8V on-die voltage regulator which powers the PCIe & DMI PLL may not be stable when powering on, causing above issues.

Implication: PLL not operating correctly could result in not detecting PCIe cards or DMI may not operate correctly, resulting in system hang and IERR# assertion.

Workaround: Motherboard designers are required to implement board changes:

- Require 1.25V through LC filter on MCH VCCAPLL_EXT (Ball A20) & VCCAPLL_EXT2 (Ball AR10).
- Require 1.25V on MCH VCC_EXP_PLL (Ball AB13).
- BIOS must disable 1.8V on-die VR. Contact your Intel field representative for the latest BIOS information.

Status: No Fix. For affected steppings, see the Summary Table of Changes.

## 3. IERR due to DMI/PCIe Link Not Trained

Problem: The MCH has a rare meta-stability condition within the DMI/primary PCIe and secondary PCIe receiver PLL divider circuitry. The MCH DMI/primary PCIe receiver may not be locked at the correct internal clock phase during warm or cold reset - causing the DMI/primary PCIe link to not train. The MCH secondary PCIe receiver may not be locked - causing the secondary PCIe link to not train. Each lock independently. If the DMI/PCIe receiver divider locked the correct clock phase, the receiver divider stays locked - and the link stays trained - until the next warm or cold reset.

Implication:

- If the rare meta-stability condition occurs, the processor may assert IERR due to traffic across the DMI link not completing. If the ICH Watch Dog Timer is enabled, the timer will time out and reboot the system. On the subsequent reset, the DMI/primary PCIe receiver may lock at the correct phase - and normal operation continues.

- In the extremely rare event that meta-stability occurs on back-to-back resets, the system could hang due to the DMI link not being trained. The Watch Dog Timer has timed out once, and would not timeout again to reboot the system. Intel has not observed the occurence of back-to-back meta-stable conditions.
- If the rare meta-stability condition occurs when the system is in ACPI S3 state, data saved in memory may be lost.
- If the rare meta-stability condition occurs on the secondary PCIe receiver PLL divider circuity, a PCIe add-in card present in the slot would not be trained.

Workaround:

- BIOS enable ICH Watch Dog Tiimer.
- If a PCIe add-in card is present but not trained, the BIOS resets the secondary PCIe link to retrain the card. See latest Intel® X38 Express Chipset Family and 3200/ 3210 Chipset Family BIOS Specification.
- There is no workaround for S3. However, the occurence of this meta-stability condition during resume from S3 is rare.

Status: No Fix.

# 6 Specification Changes

There are no Specification Changes in this Specification Update revision.

# 7 Specification Clarifications

There are no Specification Clarifications in this Specification Update revision.

# 8 Documentation Changes

### 1. Error Checking and Correction

Update the Syndrome Table in the "Error Checking and Correction" Section with the following:

*<Insert Table #> is used to calculate the syndrome. Numbers in parentheses indicate the data content of that bit position. For example, bit position 36 holds the data originally in data bit 32.*

**<Insert Table #> Syndrome Bit Values**

| Syndrome | Byte |
|---|---|
| 1C | 0 |
| A2 | 1 |
| 51 | 2 |
| E | 3 |
| 94 | 4 |
| 68 | 5 |
| 43 | 6 |
| F1 | 7 |
| C1 | 8 |
| 2A | 9 |
| 15 | 10 |
| E0 | 11 |
| 49 | 12 |
| 86 | 13 |
| 34 | 14 |
| 1F | 15 |

**<Insert Table #> Syndrome Bit Values**

| Syndrome | Byte |
|---|---|
| 2C | 16 |
| A4 | 17 |
| 52 | 18 |
| D0 | 19 |
| 98 | 20 |
| 61 | 21 |
| 83 | 22 |
| 2F | 23 |
| C2 | 24 |
| 4A | 25 |
| 25 | 26 |
| D | 27 |
| 89 | 28 |
| 16 | 29 |
| 38 | 30 |
| F2 | 31 |
| 4C | 32 |
| A8 | 33 |
| 54 | 34 |
| F8 | 35 |
| B | 36 |
| 91 | 37 |
| 62 | 38 |
| 23 | 39 |
| C4 | 40 |
| 8A | 41 |
| 45 | 42 |
| 8F | 43 |
| B0 | 44 |
| 19 | 45 |
| 26 | 46 |
| 32 | 47 |
| 8C | 48 |
| A1 | 49 |
| 58 | 50 |
| 4F | 51 |
| 70 | 52 |
| 92 | 53 |

**<Insert Table #> Syndrome Bit Values**

| Syndrome | Byte |
|---|---|
| 64 | 54 |
| 13 | 55 |
| C8 | 56 |
| 1A | 57 |
| 85 | 58 |
| F4 | 59 |
| 7 | 60 |
| 29 | 61 |
| 46 | 62 |
| 31 | 63 |

Every data bit appears in either exactly 3 or exactly 5 check bit and syndrome bit equations. Every check bit appears en exactly 1 syndrome bit equation. This leads to six cases.

1. If the data comes back exactly as it was written, then the calculated check byte will match the stored check byte, and the syndrome will be all 0s.
2. If exactly one check bit is flipped between the time it is written and the time it is read back, then the syndrome will contain exactly one 1. Since the check byte is not returned to the requesting agent, no action is necessary.
3. If exactly one data bit is flipped between the time it is written and the time it is read back, then the syndrome will contain either exactly three 1s or exactly five 1s. The syndrome can then be decoded as a pointer to the bit that flipped using the same check byte generation table in reverse. If the syndrome contains 1s that match the locations of all three or all five Xs in a given row, then that is the bit which should be flipped before the QWord is returned to the requesting agent.
4. If exactly two bits flipped, there will be a nonzero even number of 1s in the syndrome. It cannot be determined which bits flipped based on that syndrome, but a multi-bit error will be recorded along with the address at which the error occurred. In addition, bits 0 and 31 of each DWord are forced to 0 in the returned data in case this read was a TLB fetch. This ensures that the table entry is invalid, such that additional data corruption can be avoided.
5. If an even number of bits greater than two flipped, there will be an even number of 1s in the syndrome, but that even number could be zero, such that detection of this scenario is not ensured. If the syndrome contains a nonzero number of 1s, it cannot be distinguished from scenario 4 above.
6. It is possible for an odd number of bits greater than one to flip between the time the data is written and the time it is read back. This scenario will always be detected, but the resulting syndrome could appear to be a multi-bit error treated similarly to scenario 4, or it could be misinterpreted as a single bit error indistinguishable from scenario 2. The data cannot be corrected, though if it appears to be a single-bit error, the algorithm will flip the bit that corresponds to the syndrome generated, thus an additional bit may be corrupted.

   Fortunately, soft error rates are low enough that it is extremely unlikely that there would be more than one soft error in the same QWord, so scenarios 5 and 6 are very rare.

## 2. DDR3 ECC Support

In Section 1.2.2 System Memory Interface of the Intel® X38 Express Chipset Datasheet, add:

- Supports both un-buffered ECC and non-ECC DDR2 or ECC and non-ECC DDR3 DIMMs.

## 3. DDR3 (ECC)XOR Chains

| Pin Count | Ball # | Chain 0 | Index |
|---|---|---|---|
| | M21 | ALLZTEST | 1509 |
| | | | |
| 1 | B39 | FSB_DB_56 | 1941 |
| 2 | D44 | FSB_DB_52 | 1846 |
| 3 | B42 | FSB_DB_55 | 1938 |
| 4 | D39 | FSB_DB_57 | 1851 |
| 5 | C42 | FSB_DB_51 | 1893 |
| 6 | C36 | FSB_DB_58 | 1899 |
| 7 | A38 | FSB_DB_49 | 1987 |
| 8 | B35 | FSB_DB_62 | 1945 |
| 9 | D38 | FSB_DB_54 | 1852 |
| 10 | E41 | FSB_DB_50 | 1804 |
| 11 | D43 | FSB_DB_53 | 1847 |
| 12 | D36 | FSB_DB_59 | 1854 |
| 13 | E35 | FSB_DB_63 | 1810 |
| 14 | E37 | FSB_DB_61 | 1808 |
| 15 | F35 | FSB_DB_48 | 1765 |
| 16 | C37 | FSB_DB_60 | 1898 |
| 17 | F33 | FSB_DB_26 | 1767 |
| 18 | B43 | FSB_DB_18 | 1937 |
| 19 | F39 | FSB_DB_17 | 1761 |
| 20 | F38 | FSB_DB_16 | 1762 |
| 21 | H33 | FSB_DB_25 | 1677 |
| 22 | G36 | FSB_DB_22 | 1719 |
| 23 | G38 | FSB_DB_20 | 1717 |
| 24 | G35 | FSB_DB_23 | 1720 |
| 25 | L36 | FSB_DB_19 | 1539 |
| 26 | L33 | FSB_DB_29 | 1542 |
| 27 | L34 | FSB_DB_27 | 1541 |
| 28 | N33 | FSB_DB_28 | 1452 |
| 29 | N31 | FSB_DB_30 | 1454 |
| 30 | K34 | FSB_DB_24 | 1586 |
| 31 | M31 | FSB_DB_31 | 1499 |
| 32 | K35 | FSB_DB_21 | 1585 |
| 33 | L24 | FSB_DB_44 | 1551 |
| 34 | H24 | FSB_DB_45 | 1686 |
| 35 | G24 | FSB_DB_47 | 1731 |
| 36 | K28 | FSB_DB_40 | 1592 |
| 37 | K24 | FSB_DB_46 | 1596 |
| 38 | F31 | FSB_DB_32 | 1769 |
| 39 | L30 | FSB_DB_36 | 1545 |
| 40 | G30 | FSB_DB_38 | 1725 |
| 41 | N24 | FSB_DB_42 | 1461 |
| 42 | H31 | FSB_DB_34 | 1679 |
| 43 | H30 | FSB_DB_39 | 1680 |
| 44 | L28 | FSB_DB_41 | 1547 |
| 45 | M30 | FSB_DB_35 | 1500 |
| 46 | N30 | FSB_DB_37 | 1455 |
| 47 | K31 | FSB_DB_33 | 1589 |
| 48 | L25 | FSB_DB_43 | 1550 |
| 49 | E42 | FSB_DB_15 | 1803 |
| 50 | F41 | FSB_DB_14 | 1759 |
| 51 | G42 | FSB_DB_11 | 1713 |
| 52 | G44 | FSB_DB_13 | 1711 |
| 53 | H42 | FSB_DB_9 | 1668 |
| 54 | J43 | FSB_DB_8 | 1622 |
| 55 | H45 | FSB_DB_12 | 1665 |
| 56 | L42 | FSB_DB_7 | 1533 |
| 57 | M45 | FSB_DB_5 | 1485 |
| 58 | M42 | FSB_DB_3 | 1488 |
| 59 | L44 | FSB_DB_6 | 1531 |
| 60 | J41 | FSB_DB_10 | 1624 |
| 61 | P42 | FSB_DB_0 | 1398 |
| 62 | N41 | FSB_DB_1 | 1444 |
| 63 | N42 | FSB_DB_4 | 1443 |
| 64 | N44 | FSB_DB_2 | 1441 |

| Pin Count | Ball # | Chain 1 | Index |
|---|---|---|---|
| | L22 | XORTEST | 1553 |
| | | | |
| 1 | H39 | FSB_REQB_4 | 1671 |
| 2 | K42 | FSB_AB_15 | 1578 |
| 3 | G40 | FSB_REQB_1 | 1715 |
| 4 | K36 | FSB_REQB_3 | 1584 |
| 5 | F43 | FSB_AB_3 | 1757 |
| 6 | M36 | FSB_AB_5 | 1494 |
| 7 | K38 | FSB_AB_6 | 1582 |
| 8 | M38 | FSB_AB_4 | 1492 |
| 9 | L40 | FSB_AB_7 | 1535 |
| 10 | C44 | FSB_REQB_0 | 1891 |
| 11 | M40 | FSB_ADSTBB_0 | 1490 |
| 12 | N40 | FSB_AB_9 | 1445 |
| 13 | L39 | FSB_REQB_2 | 1536 |
| 14 | N36 | FSB_AB_8 | 1449 |
| 15 | N39 | FSB_AB_11 | 1446 |
| 16 | N38 | FSB_AB_13 | 1447 |
| 17 | R35 | FSB_AB_16 | 1360 |
| 18 | N34 | FSB_AB_12 | 1451 |
| 19 | R39 | FSB_AB_14 | 1356 |
| 20 | R36 | FSB_AB_10 | 1359 |
| 21 | T34 | FSB_AB_19 | 1316 |
| 22 | P43 | FSB_AB_21 | 1397 |
| 23 | T40 | FSB_AB_17 | 1310 |
| 24 | W34 | FSB_AB_25 | 1181 |
| 25 | W36 | FSB_AB_30 | 1179 |
| 26 | T38 | FSB_AB_20 | 1312 |
| 27 | V35 | FSB_AB_26 | 1225 |
| 28 | W33 | FSB_AB_27 | 1182 |
| 29 | W38 | FSB_AB_22 | 1177 |
| 30 | V34 | FSB_ADSTBB_1 | 1226 |
| 31 | AA33 | FSB_AB_31 | 1092 |
| 32 | T36 | FSB_AB_18 | 1314 |
| 33 | AB35 | FSB_AB_34 | 1045 |
| 34 | AA35 | FSB_AB_32 | 1090 |
| 35 | V38 | FSB_AB_23 | 1222 |
| 36 | AB34 | FSB_AB_29 | 1046 |
| 37 | V39 | FSB_AB_24 | 1221 |
| 38 | AA40 | FSB_AB_33 | 1085 |
| 39 | V43 | FSB_AB_28 | 1217 |
| 40 | AA38 | FSB_AB_35 | 1087 |

| Pin Count | Ball # | Chain 2 | Index |
|---|---|---|---|
| | P16 | ICH_SYNCB | 1424 |
| | | | |
| 1 | G34 | FSB_DSTBNB_1 | 1721 |
| 2 | H34 | FSB_DSTBPB_1 | 1676 |
| 3 | W41 | FSB_RSB_1 | 1174 |
| 4 | R42 | FSB_HITB | 1353 |
| 5 | W40 | FSB_TRDYB | 1175 |
| 6 | V42 | FSB_HITMB | 1218 |
| 7 | M25 | FSB_DSTBNB_2 | 1505 |
| 8 | N25 | FSB_DSTBPB_2 | 1460 |
| 9 | K43 | FSB_DSTBNB_0 | 1577 |
| 10 | J44 | FSB_DSTBPB_0 | 1621 |
| 11 | T45 | FSB_LOCKB | 1305 |
| 12 | U42 | FSB_BNRB | 1263 |
| 13 | H38 | FSB_BPRIB | 1672 |
| 14 | D35 | FSB_CPURSTB | 1855 |

| Pin Count | Ball # | Chain 3 | Index |
|---|---|---|---|
| | N18 | RSVD | 1467 |
| | | | |
| 1 | D41 | FSB_DSTBNB_3 | 1849 |
| 2 | C40 | FSB_DSTBPB_3 | 1895 |
| 3 | B37 | FSB_DINVB_3 | 1943 |
| 4 | E40 | FSB_DINVB_1 | 1805 |
| 5 | T39 | FSB_DEFERB | 1311 |
| 6 | R44 | FSB_RSB_0 | 1351 |
| 7 | U41 | FSB_DRDYB | 1264 |
| 8 | T42 | FSB_DBSYB | 1308 |
| 9 | R41 | FSB_RSB_2 | 1354 |
| 10 | N28 | FSB_DINVB_2 | 1457 |
| 11 | L41 | FSB_DINVB_0 | 1534 |
| 12 | W44 | FSB_BREQ0B | 1171 |
| 13 | U44 | FSB_ADSB | 1261 |

| Pin Count | Ball # | Chain 4 | Index |
|---|---|---|---|
| | AN12 | RSVD | 573 |
| | | | |
| 1 | AK35 | DDR_A_CB_3 | 685 |
| 2 | AL33 | DDR_A_CB_0 | 642 |
| 3 | AK34 | DDR_A_CB_6 | 686 |
| 4 | AK33 | DDR_A_CB_4 | 687 |
| 5 | AK39 | DDR_A_CB_7 | 681 |
| 6 | AN35 | DDR_A_CB_1 | 550 |
| 7 | AL34 | DDR_A_CB_5 | 641 |
| 8 | AK38 | DDR_A_CB_2 | 682 |
| 9 | AY41 | DDR_A_ODT_1 | 229 |
| 10 | BB39 | DDR_A_CSB_1 | 141 |
| 11 | BD42 | DDR_A_CSB_0 | 48 |
| 12 | BB44 | DDR3_A_CSB1 | 136 |
| 13 | BD37 | DDR_A_MA_10 | 53 |
| 14 | BB43 | DDR_A_ODT_0 | 137 |
| 15 | BD35 | DDR3_A_MA0 | 55 |
| 16 | BC36 | DDR_A_MA_0 | 99 |
| 17 | BA27 | DDR_A_MA_9 | 198 |
| 18 | BB30 | DDR_A_MA_2 | 150 |
| 19 | BB29 | DDR_A_MA_3 | 151 |
| 20 | BA29 | DDR_A_MA_4 | 196 |
| 21 | AV35 | DDR_A_CKB_2 | 325 |
| 22 | AT34 | DDR_A_CK_2 | 416 |
| 23 | AT33 | DDR_A_CK_0 | 417 |
| 24 | AN28 | DDR_A_CK_1 | 557 |
| 25 | AR33 | DDR_A_CKB_0 | 462 |
| 26 | AM28 | DDR_A_CKB_1 | 602 |
| 27 | BD29 | DDR_A_MA_6 | 61 |
| 28 | BB31 | DDR_A_MA_1 | 149 |
| 29 | BB28 | DDR_A_MA_5 | 152 |
| 30 | BC28 | DDR_A_MA_8 | 107 |
| 31 | AY27 | DDR_A_MA_7 | 243 |
| 32 | AY24 | DDR_A_CKE_0 | 246 |
| 33 | BB25 | DDR_A_CKE_1 | 155 |
| 34 | AV21 | DDR_A_DQSB_3 | 339 |
| 35 | AP21 | DDR_A_DM_3 | 519 |
| 36 | AY15 | DDR_A_DQSB_2 | 255 |
| 37 | BC14 | DDR_A_DM_2 | 121 |
| 38 | AY11 | DDR_A_DQSB_1 | 259 |
| 39 | BC10 | DDR_A_DM_1 | 125 |
| 40 | BC6 | DDR_A_DQSB_0 | 129 |
| 41 | BB5 | DDR_A_DM_0 | 175 |

| Pin Count | Ball # | Chain 5 | Index |
|---|---|---|---|
| | AM14 | RSVD | 616 |
| | | | |
| 1 | AA44 | DDR_A_DQSB_7 | 1081 |
| 2 | AB40 | DDR_A_DM_7 | 1040 |
| 3 | AD42 | DDR_A_DQSB_6 | 948 |
| 4 | AE44 | DDR_A_DM_6 | 901 |
| 5 | AL36 | DDR_A_DQSB_8 | 639 |
| 6 | AM42 | DDR_A_DQSB_5 | 588 |
| 7 | AN44 | DDR_A_DM_5 | 541 |
| 8 | AT42 | DDR_A_DQSB_4 | 408 |
| 9 | AU44 | DDR_A_DM_4 | 361 |
| 10 | BA42 | DDR_A_MA_13 | 183 |
| 11 | BB41 | DDR_A_CASB | 139 |
| 12 | BD39 | DDR_A_WEB | 51 |
| 13 | BB36 | DDR_A_BS_1 | 144 |
| 14 | BC40 | DDR3_A_WEB | 95 |
| 15 | BB38 | DDR_A_RASB | 142 |
| 16 | BC37 | DDR_A_BS_0 | 98 |
| 17 | BA25 | DDR_A_MA_14 | 200 |
| 18 | BD27 | DDR_A_MA_11 | 63 |
| 19 | BB26 | DDR_A_BS_2 | 154 |
| 20 | BB27 | DDR_A_MA_12 | 153 |
| 21 | AK15 | CL_DATA | 705 |
| 22 | AK14 | CL_CLK | 706 |

| Pin Count | Ball # | Chain 6 | Index |
|---|---|---|---|
| | F21 | BSEL1 | 1779 |
| | | | |
| 1 | AA42 | DDR_A_DQS_7 | 1083 |
| 2 | Y42 | DDR_A_DQ_58 | 1128 |
| 3 | AA41 | DDR_A_DQ_62 | 1084 |
| 4 | AB42 | DDR_A_DQ_56 | 1038 |
| 5 | AB43 | DDR_A_DQ_57 | 1037 |
| 6 | W42 | DDR_A_DQ_59 | 1173 |
| 7 | AC40 | DDR_A_DQ_60 | 995 |
| 8 | Y45 | DDR_A_DQ_63 | 1125 |
| 9 | AB39 | DDR_A_DQ_61 | 1041 |
| 10 | AD43 | DDR_A_DQS_6 | 947 |
| 11 | AC42 | DDR_A_DQ_50 | 993 |
| 12 | AC39 | DDR_A_DQ_55 | 996 |
| 13 | AE41 | DDR_A_DQ_48 | 904 |
| 14 | AD40 | DDR_A_DQ_54 | 950 |
| 15 | AC45 | DDR_A_DQ_51 | 990 |
| 16 | AF42 | DDR_A_DQ_52 | 858 |
| 17 | AF45 | DDR_A_DQ_53 | 855 |
| 18 | AE42 | DDR_A_DQ_49 | 903 |
| 19 | AL38 | DDR_A_DQS_8 | 637 |
| 20 | AM43 | DDR_A_DQS_5 | 587 |
| 21 | AL40 | DDR_A_DQ_46 | 635 |
| 22 | AN41 | DDR_A_DQ_40 | 544 |
| 23 | AN42 | DDR_A_DQ_41 | 543 |
| 24 | AP42 | DDR_A_DQ_44 | 498 |
| 25 | AL41 | DDR_A_DQ_47 | 634 |
| 26 | AP45 | DDR_A_DQ_45 | 495 |
| 27 | AL42 | DDR_A_DQ_43 | 633 |
| 28 | AL44 | DDR_A_DQ_42 | 631 |
| 29 | AT43 | DDR_A_DQS_4 | 407 |
| 30 | AU43 | DDR_A_DQ_33 | 362 |
| 31 | AU41 | DDR_A_DQ_37 | 364 |
| 32 | AV42 | DDR_A_DQ_32 | 318 |
| 33 | AR41 | DDR_A_DQ_38 | 454 |
| 34 | AR40 | DDR_A_DQ_39 | 455 |
| 35 | AR44 | DDR_A_DQ_34 | 451 |
| 36 | AW42 | DDR_A_DQ_36 | 273 |
| 37 | AR42 | DDR_A_DQ_35 | 453 |
| 38 | AT21 | DDR_A_DQS_3 | 429 |
| 39 | AY21 | DDR_A_DQ_25 | 249 |
| 40 | AW19 | DDR_A_DQ_29 | 296 |
| 41 | AN21 | DDR_A_DQ_30 | 564 |
| 42 | AW22 | DDR_A_DQ_31 | 293 |
| 43 | AT22 | DDR_A_DQ_27 | 428 |
| 44 | AN22 | DDR_A_DQ_26 | 563 |
| 45 | AN19 | DDR_A_DQ_24 | 566 |
| 46 | AV19 | DDR_A_DQ_28 | 341 |
| 47 | BA15 | DDR_A_DQS_2 | 210 |
| 48 | BB16 | DDR_A_DQ_18 | 164 |
| 49 | BD15 | DDR_A_DQ_22 | 75 |
| 50 | BE16 | DDR_A_DQ_19 | 29 |
| 51 | BB14 | DDR_A_DQ_17 | 166 |
| 52 | BB15 | DDR_A_DQ_23 | 165 |
| 53 | BA13 | DDR_A_DQ_20 | 212 |
| 54 | BD13 | DDR_A_DQ_16 | 77 |
| 55 | BB13 | DDR_A_DQ_21 | 167 |
| 56 | BA11 | DDR_A_DQS_1 | 214 |
| 57 | BC9 | DDR_A_DQ_13 | 126 |
| 58 | BD11 | DDR_A_DQ_14 | 79 |
| 59 | BB11 | DDR_A_DQ_15 | 169 |
| 60 | BE12 | DDR_A_DQ_11 | 33 |
| 61 | BD9 | DDR_A_DQ_8 | 81 |
| 62 | BA9 | DDR_A_DQ_12 | 216 |
| 63 | BB12 | DDR_A_DQ_10 | 168 |
| 64 | BB10 | DDR_A_DQ_9 | 170 |
| 65 | BA6 | DDR_A_DQS_0 | 219 |
| 66 | BB7 | DDR_A_DQ_7 | 173 |
| 67 | BB8 | DDR_A_DQ_2 | 172 |
| 68 | BE8 | DDR_A_DQ_3 | 37 |
| 69 | BD7 | DDR_A_DQ_6 | 83 |
| 70 | BD4 | DDR_A_DQ_1 | 86 |
| 71 | BC4 | DDR_A_DQ_0 | 131 |
| 72 | BB4 | DDR_A_DQ_5 | 176 |
| 73 | BD3 | DDR_A_DQ_4 | 87 |

| Pin Count | Ball # | Chain 7 | Index |
|---|---|---|---|
| | F18 | BSEL2 | 1782 |
| | | | |
| 1 | AW44 | DDR_A_ODT_3 | 271 |
| 2 | AY43 | DDR_A_CSB_3 | 227 |
| 3 | BA41 | DDR_A_ODT_2 | 184 |
| 4 | BB39 | DDR_A_CSB_2 | 141 |
| 5 | AV31 | DDR_A_CK_3 | 329 |
| 6 | AT31 | DDR_A_CKB_3 | 419 |
| 7 | AT36 | DDR_A_CKB_5 | 414 |
| 8 | AT35 | DDR_A_CK_5 | 415 |
| 9 | AN27 | DDR_A_CK_4 | 568 |
| 10 | AM27 | DDR_A_CKB_4 | 603 |
| 11 | BC24 | DDR_A_CKE_3 | 111 |
| 12 | BB25 | DDR_A_CKE_2 | 155 |
| 13 | BB23 | DDR3_DRAMRSTB | 157 |

| Pin Count | Ball # | Chain 8 | Index |
|---|---|---|---|
| | AN13 | RSVD | 572 |
| | | | |
| 1 | AG42 | DDR_B_CB_2 | 813 |
| 2 | AG44 | DDR_B_CB_7 | 811 |
| 3 | AG41 | DDR_B_CB_6 | 814 |
| 4 | AK45 | DDR_B_CB_0 | 675 |
| 5 | AJ42 | DDR_B_CB_4 | 723 |
| 6 | AG40 | DDR_B_CB_3 | 815 |
| 7 | AJ44 | DDR_B_CB_1 | 721 |
| 8 | AK42 | DDR_B_CB_5 | 678 |
| 9 | BB34 | DDR_B_ODT_1 | 146 |
| 10 | BD33 | DDR_B_ODT_0 | 57 |
| 11 | BB35 | DDR_B_CSB_1 | 145 |
| 12 | BA31 | DDR_B_CSB_0 | 194 |
| 13 | AV30 | DDR_B_CKB_0 | 330 |
| 14 | AW30 | DDR_B_CK_0 | 285 |
| 15 | AW33 | DDR_B_CKB_2 | 282 |
| 16 | AR28 | DDR_B_CK_1 | 467 |
| 17 | AP28 | DDR_B_CKB_1 | 512 |
| 18 | AV33 | DDR_B_CK_2 | 327 |
| 19 | BB21 | DDR_B_MA_5 | 159 |
| 20 | BB22 | DDR_B_MA_2 | 158 |
| 21 | BD21 | DDR_B_MA_4 | 69 |
| 22 | BC22 | DDR_B_MA_1 | 113 |
| 23 | AW24 | DDR_B_MA_10 | 291 |
| 24 | BB20 | DDR_B_MA_6 | 160 |
| 25 | BB19 | DDR_B_MA_9 | 161 |
| 26 | BE20 | DDR_B_MA_8 | 25 |
| 27 | BA21 | DDR_B_MA_3 | 204 |
| 28 | AY19 | DDR_B_MA_7 | 251 |
| 29 | BD17 | DDR_B_CKE_0 | 73 |
| 30 | AY22 | DDR_B_MA_0 | 248 |
| 31 | BD19 | DDR_B_CKE_1 | 71 |
| 32 | AR24 | DDR_B_DQSB_3 | 471 |
| 33 | AY25 | DDR_B_DM_3 | 245 |
| 34 | AP16 | DDR_B_DQSB_2 | 524 |
| 35 | AW16 | DDR_B_DM_2 | 299 |
| 36 | AR12 | DDR_B_DQSB_1 | 483 |
| 37 | AT13 | DDR_B_DM_1 | 437 |
| 38 | AT10 | DDR_B_DQSB_0 | 440 |
| 39 | AY8 | DDR_B_DM_0 | 262 |

| Pin Count | Ball # | Chain 9 | Index |
|---|---|---|---|
| | AP12 | RSVD | 528 |
| | | | |
| 1 | AD33 | DDR_B_DQSB_7 | 957 |
| 2 | AD35 | DDR_B_DM_7 | 955 |
| 3 | AG38 | DDR_B_DQSB_6 | 817 |
| 4 | AG35 | DDR_B_DM_6 | 820 |
| 5 | AH42 | DDR_B_DQSB_8 | 768 |
| 6 | AP40 | DDR_B_DQSB_5 | 500 |
| 7 | AN36 | DDR_B_DM_5 | 549 |
| 8 | AV38 | DDR_B_DQSB_4 | 322 |
| 9 | AY40 | DDR_B_DM_4 | 230 |
| 10 | BA33 | DDR_B_MA_13 | 192 |
| 11 | BD31 | DDR_B_RASB | 59 |
| 12 | BB32 | DDR_B_CASB | 148 |
| 13 | AY31 | DDR_B_WEB | 239 |
| 14 | AY18 | DDR_B_MA_12 | 252 |
| 15 | BA19 | DDR_B_MA_11 | 206 |
| 16 | BC18 | DDR_B_MA_14 | 117 |
| 17 | BB18 | DDR_B_BS_2 | 162 |
| 18 | BB24 | DDR_B_BS_0 | 156 |
| 19 | AW23 | DDR_B_BS_1 | 292 |

| Pin Count | Ball # | Chain 10 | Index |
|---|---|---|---|
| | K19 | EXP_SLR | 1601 |
| | | | |
| 1 | AC33 | DDR_B_DQS_7 | 1002 |
| 2 | AC36 | DDR_B_DQ_62 | 999 |
| 3 | AB32 | DDR_B_DQ_58 | 1048 |
| 4 | AB38 | DDR_B_DQ_59 | 1042 |
| 5 | AE34 | DDR_B_DQ_61 | 911 |
| 6 | AD36 | DDR_B_DQ_57 | 954 |
| 7 | AE35 | DDR_B_DQ_60 | 910 |
| 8 | AD39 | DDR_B_DQ_56 | 951 |
| 9 | AC34 | DDR_B_DQ_63 | 1001 |
| 10 | AG39 | DDR_B_DQS_6 | 816 |
| 11 | AE38 | DDR_B_DQ_51 | 907 |
| 12 | AE33 | DDR_B_DQ_55 | 912 |
| 13 | AE39 | DDR_B_DQ_50 | 906 |
| 14 | AH33 | DDR_B_DQ_52 | 777 |
| 15 | AH34 | DDR_B_DQ_48 | 776 |
| 16 | AH36 | DDR_B_DQ_53 | 774 |
| 17 | AG33 | DDR_B_DQ_49 | 822 |
| 18 | AE40 | DDR_B_DQ_54 | 905 |
| 19 | AH43 | DDR_B_DQS_8 | 767 |
| 20 | AP39 | DDR_B_DQS_5 | 501 |

Chain 10 continued

| | | | |
|---|---|---|---|
| 21 | AP35 | DDR_B_DQ_42 | 505 |
| 22 | AN39 | DDR_B_DQ_46 | 546 |
| 23 | AP36 | DDR_B_DQ_41 | 504 |
| 24 | AV36 | DDR_B_DQ_44 | 324 |
| 25 | AR34 | DDR_B_DQ_45 | 461 |
| 26 | AN40 | DDR_B_DQ_47 | 545 |
| 27 | AR36 | DDR_B_DQ_40 | 459 |
| 28 | AN33 | DDR_B_DQ_43 | 552 |
| 29 | AW39 | DDR_B_DQS_4 | 276 |
| 30 | AV39 | DDR_B_DQ_38 | 321 |
| 31 | AT40 | DDR_B_DQ_35 | 410 |
| 32 | AT38 | DDR_B_DQ_34 | 412 |
| 33 | AV40 | DDR_B_DQ_39 | 320 |
| 34 | AY39 | DDR_B_DQ_32 | 231 |
| 35 | AW38 | DDR_B_DQ_33 | 277 |
| 36 | AW36 | DDR_B_DQ_37 | 279 |
| 37 | AY38 | DDR_B_DQ_36 | 232 |
| 38 | AR25 | DDR_B_DQS_3 | 470 |
| 39 | AV27 | DDR_B_DQ_27 | 333 |
| 40 | AP27 | DDR_B_DQ_31 | 513 |
| 41 | AT25 | DDR_B_DQ_30 | 425 |
| 42 | AT27 | DDR_B_DQ_26 | 423 |
| 43 | AW25 | DDR_B_DQ_24 | 290 |
| 44 | AP24 | DDR_B_DQ_29 | 516 |
| 45 | AN24 | DDR_B_DQ_28 | 561 |
| 46 | AV25 | DDR_B_DQ_25 | 335 |
| 47 | AN18 | DDR_B_DQS_2 | 567 |
| 48 | AT19 | DDR_B_DQ_19 | 431 |
| 49 | AP19 | DDR_B_DQ_18 | 521 |
| 50 | AN16 | DDR_B_DQ_20 | 569 |
| 51 | AT18 | DDR_B_DQ_22 | 432 |
| 52 | AR18 | DDR_B_DQ_23 | 477 |
| 53 | AV16 | DDR_B_DQ_17 | 344 |
| 54 | AR16 | DDR_B_DQ_21 | 479 |
| 55 | AY16 | DDR_B_DQ_16 | 254 |
| 56 | AR13 | DDR_B_DQS_1 | 482 |
| 57 | AV15 | DDR_B_DQ_11 | 345 |
| 58 | AT15 | DDR_B_DQ_10 | 435 |
| 59 | AW13 | DDR_B_DQ_13 | 302 |
| 60 | AN15 | DDR_B_DQ_14 | 570 |
| 61 | AY13 | DDR_B_DQ_9 | 257 |
| 62 | AW12 | DDR_B_DQ_12 | 303 |
| 63 | AP15 | DDR_B_DQ_15 | 525 |
| 64 | AY12 | DDR_B_DQ_8 | 258 |
| 65 | AW10 | DDR_B_DQS_0 | 305 |
| 66 | AW8 | DDR_B_DQ_0 | 307 |
| 67 | AT11 | DDR_B_DQ_2 | 439 |
| 68 | AW11 | DDR_B_DQ_7 | 304 |
| 69 | AY7 | DDR_B_DQ_1 | 263 |
| 70 | AW6 | DDR_B_DQ_5 | 309 |
| 71 | AR11 | DDR_B_DQ_6 | 484 |
| 72 | AT12 | DDR_B_DQ_3 | 438 |
| 73 | AV8 | DDR_B_DQ_4 | 352 |

| Pin Count | Ball # | Chain 11 | Index |
|---|---|---|---|
| | L18 | EXP_EN | 1557 |
| | | | |
| 1 | AY35 | DDR_B_ODT_3 | 235 |
| 2 | BA35 | DDR_B_CSB_3 | 190 |
| 3 | BB33 | DDR_B_ODT_2 | 147 |
| 4 | BA37 | DDR3_B_ODT3 | 188 |
| 5 | BC32 | DDR_B_CSB_2 | 103 |
| 6 | AY34 | DDR_B_CKB_5 | 236 |
| 7 | AW34 | DDR_B_CK_5 | 281 |
| 8 | AY28 | DDR_B_CKB_4 | 242 |
| 9 | AY30 | DDR_B_CK_4 | 240 |
| 10 | AP31 | DDR_B_CKB_3 | 509 |
| 11 | AR31 | DDR_B_CK_3 | 464 |
| 12 | BA17 | DDR_B_CKE_3 | 208 |
| 13 | BB17 | DDR_B_CKE_2 | 163 |

| Pin Count | Ball # | Chain 13 | Index |
|---|---|---|---|
| | H21 | RSVD | 1689 |
| | | | |
| 1 | A8 | PEG_TXN_7 | 2017 |
| 2 | B7 | PEG_TXP_7 | 1973 |
| 3 | H10 | PEG_RXN_7 | 1700 |
| 4 | G10 | PEG_RXP_7 | 1745 |
| 5 | E9 | PEG_TXN_6 | 1836 |
| 6 | D8 | PEG_TXP_6 | 1882 |
| 7 | L12 | PEG_RXN_6 | 1563 |
| 8 | K11 | PEG_RXP_6 | 1609 |
| 9 | C10 | PEG_TXN_5 | 1925 |
| 10 | B9 | PEG_TXP_5 | 1971 |
| 11 | G12 | PEG_RXN_5 | 1743 |
| 12 | H12 | PEG_RXP_5 | 1698 |
| 13 | E11 | PEG_TXN_4 | 1834 |
| 14 | D10 | PEG_TXP_4 | 1880 |
| 15 | M13 | PEG_RXN_4 | 1517 |
| 16 | N13 | PEG_RXP_4 | 1472 |
| 17 | A12 | PEG_TXN_3 | 2013 |
| 18 | B11 | PEG_TXP_3 | 1969 |
| 19 | K13 | PEG_RXN_3 | 1607 |
| 20 | L13 | PEG_RXP_3 | 1562 |
| 21 | D12 | PEG_TXN_2 | 1878 |
| 22 | E13 | PEG_TXP_2 | 1832 |
| 23 | G13 | PEG_RXN_2 | 1742 |
| 24 | H13 | PEG_RXP_2 | 1697 |
| 25 | D14 | PEG_TXN_1 | 1876 |

| Pin Count | Ball # | Chain 12 | Index |
|---|---|---|---|
| | M22 | BSEL0 | 1508 |
| | | | |
| 1 | V10 | DMI_TXP_3 | 1250 |
| 2 | V11 | DMI_TXN_3 | 1249 |
| 3 | V7 | DMI_RXP_3 | 1253 |
| 4 | V6 | DMI_RXN_3 | 1254 |
| 5 | R2 | DMI_TXP_2 | 1393 |
| 6 | T1 | DMI_TXN_2 | 1349 |
| 7 | P4 | DMI_RXP_2 | 1436 |
| 8 | R5 | DMI_RXN_2 | 1390 |
| 9 | N2 | DMI_TXP_1 | 1483 |
| 10 | P3 | DMI_TXN_1 | 1437 |
| 11 | T7 | DMI_RXP_1 | 1343 |
| 12 | T8 | DMI_RXN_1 | 1342 |
| 13 | R7 | DMI_TXP_0 | 1388 |
| 14 | R6 | DMI_TXN_0 | 1389 |
| 15 | N5 | DMI_RXP_0 | 1480 |
| 16 | M4 | DMI_RXN_0 | 1526 |

| | | | |
|---|---|---|---|
| 26 | E15 | PEG_TXP_1 | 1830 |
| 27 | C14 | PEG_RXN_1 | 1921 |
| 28 | B13 | PEG_RXP_1 | 1967 |
| 29 | E17 | PEG_TXN_0 | 1828 |
| 30 | D16 | PEG_TXP_0 | 1874 |
| 31 | B15 | PEG_RXN_0 | 1965 |
| 32 | A16 | PEG_RXP_0 | 2009 |
| 33 | L2 | PEG_TXN_15 | 1573 |
| 34 | M1 | PEG_TXP_15 | 1529 |
| 35 | N10 | PEG_RXN_15 | 1475 |
| 36 | N8 | PEG_RXP_15 | 1477 |
| 37 | K4 | PEG_TXN_14 | 1616 |
| 38 | L5 | PEG_TXP_14 | 1570 |
| 39 | J2 | PEG_RXN_14 | 1663 |
| 40 | K3 | PEG_RXP_14 | 1617 |
| 41 | H4 | PEG_TXN_13 | 1706 |
| 42 | J5 | PEG_TXP_13 | 1660 |
| 43 | M8 | PEG_RXN_13 | 1522 |
| 44 | M7 | PEG_RXP_13 | 1523 |
| 45 | G2 | PEG_TXN_12 | 1753 |
| 46 | H1 | PEG_TXP_12 | 1709 |
| 47 | L10 | PEG_RXN_12 | 1565 |
| 48 | M11 | PEG_RXP_12 | 1519 |
| 49 | E4 | PEG_TXN_11 | 1841 |
| 50 | F5 | PEG_TXP_11 | 1795 |
| 51 | K8 | PEG_RXN_11 | 1612 |
| 52 | K7 | PEG_RXP_11 | 1613 |
| 53 | D3 | PEG_TXN_10 | 1887 |
| 54 | F3 | PEG_TXP_10 | 1797 |
| 55 | C2 | PEG_RXN_10 | 1933 |
| 56 | D2 | PEG_RXP_10 | 1888 |
| 57 | B4 | PEG_TXN_9 | 1976 |
| 58 | B3 | PEG_TXP_9 | 1977 |
| 59 | G6 | PEG_RXN_9 | 1749 |
| 60 | F7 | PEG_RXP_9 | 1793 |
| 61 | C4 | PEG_TXN_8 | 1931 |
| 62 | C6 | PEG_TXP_8 | 1929 |
| 63 | D5 | PEG_RXN_8 | 1885 |
| 64 | E6 | PEG_RXP_8 | 1839 |

| Pin Count | Ball # | Chain 14 | Index |
|---|---|---|---|
| | G22 | RSVD | 1733 |
| | | | |
| 1 | AJ5 | PEG2_TXN_7 | 760 |
| 2 | AK4 | PEG2_TXP_7 | 716 |
| 3 | AE11 | PEG2_RXN_7 | 934 |
| 4 | AE10 | PEG2_RXP_7 | 935 |
| 5 | AH3 | PEG2_TXN_6 | 807 |
| 6 | AJ2 | PEG2_TXP_6 | 763 |
| 7 | AD12 | PEG2_RXN_6 | 978 |
| 8 | AE13 | PEG2_RXP_6 | 932 |
| 9 | AG5 | PEG2_TXN_5 | 850 |
| 10 | AH4 | PEG2_TXP_5 | 806 |
| 11 | AC7 | PEG2_RXN_5 | 1028 |
| 12 | AC6 | PEG2_RXP_5 | 1029 |
| 13 | AF1 | PEG2_TXN_4 | 899 |
| 14 | AG2 | PEG2_TXP_4 | 853 |
| 15 | AC10 | PEG2_RXN_4 | 1025 |
| 16 | AC11 | PEG2_RXP_4 | 1024 |
| 17 | AE5 | PEG2_TXN_3 | 940 |
| 18 | AF4 | PEG2_TXP_3 | 896 |
| 19 | AB12 | PEG2_RXN_3 | 1068 |
| 20 | AC13 | PEG2_RXP_3 | 1022 |
| 21 | AD3 | PEG2_TXN_2 | 987 |
| 22 | AE2 | PEG2_TXP_2 | 943 |
| 23 | AA7 | PEG2_RXN_2 | 1118 |
| 24 | AA6 | PEG2_RXP_2 | 1119 |
| 25 | AC4 | PEG2_TXN_1 | 1031 |
| 26 | AD4 | PEG2_TXP_1 | 986 |
| 27 | AA11 | PEG2_RXN_1 | 1114 |
| 28 | AA10 | PEG2_RXP_1 | 1115 |
| 29 | AB1 | PEG2_TXN_0 | 1079 |
| 30 | AB3 | PEG2_TXP_0 | 1077 |
| 31 | AA13 | PEG2_RXN_0 | 1112 |
| 32 | W12 | PEG2_RXP_0 | 1203 |
| 33 | AP6 | PEG2_TXN_15 | 534 |
| 34 | AP7 | PEG2_TXP_15 | 533 |
| 35 | AP11 | PEG2_RXN_15 | 529 |
| 36 | AP10 | PEG2_RXP_15 | 530 |
| 37 | AT3 | PEG2_TXN_14 | 447 |
| 38 | AU2 | PEG2_TXP_14 | 403 |
| 39 | AL7 | PEG2_RXN_14 | 668 |
| 40 | AL6 | PEG2_RXP_14 | 669 |
| 41 | AR5 | PEG2_TXN_13 | 490 |
| 42 | AT4 | PEG2_TXP_13 | 446 |
| 43 | AL10 | PEG2_RXN_13 | 665 |
| 44 | AL11 | PEG2_RXP_13 | 664 |
| 45 | AP1 | PEG2_TXN_12 | 539 |
| 46 | AR2 | PEG2_TXP_12 | 493 |
| 47 | AK13 | PEG2_RXN_12 | 707 |
| 48 | AK12 | PEG2_RXP_12 | 708 |
| 49 | AN5 | PEG2_TXN_11 | 580 |
| 50 | AP4 | PEG2_TXP_11 | 536 |
| 51 | AH6 | PEG2_RXN_11 | 804 |
| 52 | AH7 | PEG2_RXP_11 | 803 |
| 53 | AM3 | PEG2_TXN_10 | 627 |
| 54 | AN2 | PEG2_TXP_10 | 583 |
| 55 | AH10 | PEG2_RXN_10 | 800 |
| 56 | AH11 | PEG2_RXP_10 | 799 |
| 57 | AL5 | PEG2_TXN_9 | 670 |
| 58 | AM4 | PEG2_TXP_9 | 626 |
| 59 | AH13 | PEG2_RXN_9 | 797 |
| 60 | AG12 | PEG2_RXP_9 | 843 |
| 61 | AK1 | PEG2_TXN_8 | 719 |
| 62 | AL2 | PEG2_TXP_8 | 673 |
| 63 | AE6 | PEG2_RXN_8 | 939 |
| 64 | AE7 | PEG2_RXP_8 | 938 |

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