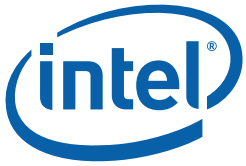

Intel® G35 Express Chipset

Specification Update

— For the Intel® 82G35 Graphics and Memory Controller Hub (GMCH)

August 2007

Notice: The Intel® 82G35 GMCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 317608-001

Contents

Revision History

Revision	Description	Date
-001	• Initial release	August 2007

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Number/Location
Intel® G35 Express Chipset Datasheet	317607-001

Nomenclature

Errata are design defects or errors. Errata may cause the Intel® 82G35 GMCH's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.

Row

Shaded:	This item is either new or modified from the previous version of the document.

NO.	E0	PLANS	ERRATA
1	X	NoFix	Data Recovery Clock (DRC) Lock-Up
2	X	NoFix	VGA Engine Hangs with Upper-left Centering Mode
3	X	NoFix	ME Warm Reset Hang
4	X	NoFix	Visual Corruption with Integrated Graphics & Intel® Flex Memory Technology Enabled using Microsoft* Vista.

Number	SPECIFICATION CHANGES
	There are no Specification Changes in this Specification Update revision.

Number	SPECIFICATION CLARIFICATIONS
	There are no Specification Clarifications in this Specification Update revision.

Number	DOCUMENTATION CHANGES
	There are no Documentation Changes in this Specification Update revision.

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Identification Information

Component Identification via Programming Interface

The Intel 82G35 GMCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
E0	8086h	2980h	03h

NOTES:

1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel 82G35 GMCH may be identified by the following component markings:

Stepping	Product	S-Spec	Lead / PbFree	Top Marking	Notes
E0	GMCH	SLAJJ	PbFree	LE82G35	Production

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Errata

1. Data Recovery Clock (DRC) Lock-Up

Problem: The PCI Express* interface Data Recovery Clock (DRC) state-machine inside the MCH on rare occasions may come up in an invalid state when the PCI Express* link is disabled and then re-enabled on Intel® G35 Express chipset based platforms.

Implication: On rare occasions when performing S1 ACPI stress test cycling on an Intel® 965/946 Express Chipset platform, the system may experience abnormal behavior such as correctable bit errors, system hang, or a blank screen.

- Scenario #1- S1 ACPI stress test cycling with an PCI Express* device that supports L1 Link Power Management inserted into the x16 PCI Express* slot.
- Scenario #2- Force x1 Algorithm invoked by system BIOS when using a x4 or x8 PCI Express* card of any class code, or a non-graphics x16 PCI Express* in the x16 PCI Express* card slot.

Workaround: Scenario #1 - Disable S1 ACPI Power Management support via BIOS, OR ensure L1 PCI Express* link power management is not supported by the PCI Express* card inserted into the x16 PCI Express* card slot. Scenario #2 - Remove Force x1 algorithm from BIOS when using a x4 or x8 PCI Express* card of any class code, or a non-graphics x16 PCI Express* in the x16 PCI Express* card slot. For the latest BIOS information, contact your Intel field representative.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

2. VGA Engine Hangs with Upper-left Centering Mode

Problem: On an Intel® G35 based platform, when launching some legacy 2D DOS applications that use non-standard VGA programming on a monitor that requires panel fitting/scaling using upper-left centering mode abnormal system behavior is observed.

Notes:

Non-standard programming refers to applications that program the VGA timing registers in a manner that the “vertical display enable end” value is greater than the “vertical blank start” value.

- The “vertical display enable end” value specifies the number of scan lines that form the vertical active display area. This is the value programmed in VGA registers CR12 bits 7 through 0 and CR07 bits 6 and 1.
- The “vertical blank start” specifies the beginning of the vertical blanking period relative to the beginning of the active display area of the screen. This is the value programmed in VGA registers CR12 bits 7 through 0, CR09 bit 5, and CR07 bit 3.

Implication: The display monitor may blank screen and the system hang. Note: Native VGA mode on CRT’s or Flat Panels operates as intended.

Workaround: None

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

3. ME Warm Reset Hang

Problem: If the default setting for the “Minimum Power-down exit to Non-Read command spacing” (sd0_cr_txp in register MCHBAR 0x260[13:10]) is programmed, Intel® G35 Express Chipset family based platforms will violate the JEDEC tXSNR timing specification during self refresh exit when Intel® Management Engine is enabled.

Implication: Depending on DIMM sensitivity to tXSNR timing violations, on rare occasions the system may experience abnormal system behavior upon resuming from warm resets and ACPI S3 state when Intel® Management Engine is enabled for Intel® Active Management Technology, Intel® Quiet System Technology, or Alert Standard Format (ASF).

Workaround: BIOS workaround – Contact your Intel field representative for the latest BIOS information.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

4. Visual Corruption with Integrated Graphics and Intel® Flex Memory Technology Enabled using Microsoft* Vista

Problem: Visual corruption is observed with the Intel® 3 Series GMCHs using new Microsoft* Vista paging model when Intel® Flex Memory Technology is enabled in the Dual Channel Asymmetric Configuration.

Implication: Visual graphics corruption on the display when running 3D applications.

Workaround: Use latest Intel® Graphics Driver (Revision 15.4.3 or newer)

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

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Specification Changes

There are no Specification Changes in this Specification Update revision.

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Specification Clarifications

There are no specification clarifications in this Specification Update revision.

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Documentation Changes

There are no documentation changes in this Specification Update revision.

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