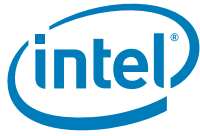


Intel[®] 6400/6402 Advanced Memory Buffer

Specification Update

October 2006



INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The Intel® 6400/6402 Advanced Memory Buffer may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Intel and the Intel logo are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

*Other names and brands may be claimed as the property of others.

Copyright © 2004-2006, Intel Corporation



Contents

1	Revision History	5
2	Preface	6
	2.1 Related Documents	6
	2.2 Nomenclature	6
3	Identification Information	7
	3.1 Intel® 6400/6402 Advanced Memory Buffer Package Markings.....	7
4	Summary Table of Changes	8
	4.1 Codes Used in Summary Table	8
	4.2 Errata	8
	4.3 Specification Changes	8
	4.4 Specification Clarifications	8
	4.5	8
	4.6 Specification Changes	9
5	Errata	10
6	Specification Changes	11





1 Revision History

Version	Description	Date
-001	<ul style="list-style-type: none">Initial release.	May 2006
-002	<ul style="list-style-type: none">Added D-1 information and Specification Update 1. Updated Errata 1 and 2.	October 2006



2 Preface

This is an update to the specifications in the documents listed in the “[Related Documents](#)” table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and software developers.

Information types defined in the [Nomenclature](#) section of this document are consolidated into this document and are no longer published in other documents. This document may also contain previously unpublished information.

2.1 Related Documents

Document Title	Document Number
<i>RS - Intel® 6400/6402 Advanced Memory Buffer Datasheet</i>	313072

2.2 Nomenclature

S-Spec Number is a five-digit code used to identify products. Products are differentiated by their unique characteristics, e.g., core speed, L3 cache size, package type, etc. as described in the processor identification information table. Read all notes associated with each S-Spec number.

ODF Number is a several digit code used to distinguish between engineering samples. These samples are used for qualification and early design validation. The functionality of these parts can range from mechanical only to fully functional.

Errata are design defects or errors. These may cause the Intel® 6400/6402 Advanced Memory Buffer’s behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes/Clarifications are modifications to the current published specifications. These changes will be incorporated in the next release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in the next release of the specification.

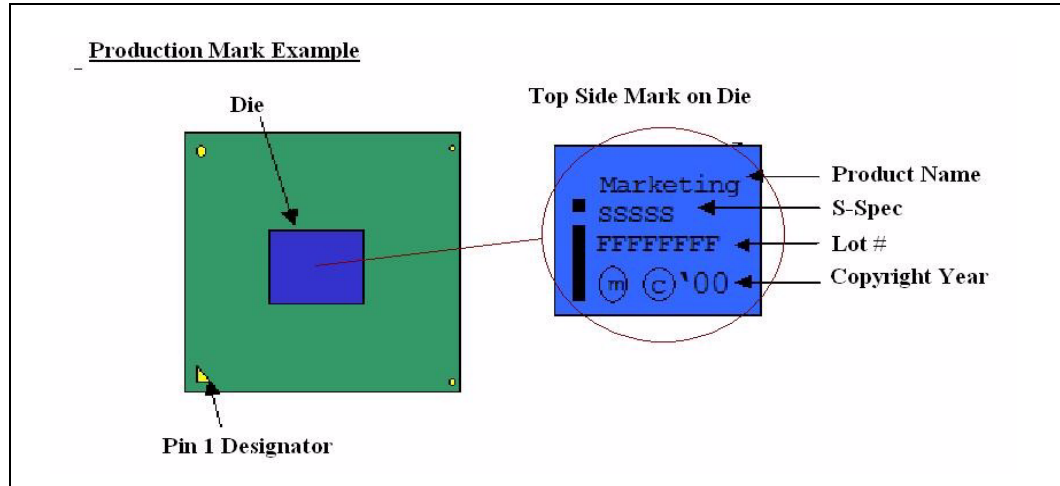
Note: Errata remain in the specification update throughout the product’s life cycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation.



3 Identification Information

3.1 Intel® 6400/6402 Advanced Memory Buffer Package Markings

Figure 3-1. Top-Side Package Marking Example



The Intel 6400/6402 Advanced Memory Buffer component can be identified by the following component markings:

AMB	Stepping	S-Spec	Notes
6402	C-0	SL9GF	2
6400	C-0	SL96G	1
6402	D-1	SL9XC	2, 3

Notes:

1. These components meet the JEDEC power specifications for 533 MHz frequencies only.
2. These components meet the JEDEC power specifications for 533 and 667 MHz frequencies.
3. These components do not support some optional registers. See Specification Change 1.



4 Summary Table of Changes

The tables included in this section indicate the errata, specification changes, specification clarifications, and documentation changes that apply to the Intel 6400/6402 Advanced Memory Buffer. Intel may fix some errata in a future stepping of the component, and account for other outstanding issues through documentation or specification changes as noted.

4.1 Codes Used in Summary Table

Stepping/Version

X: Applies to this stepping.

Blank: Fixed in listed stepping or does not exist in listed stepping.

Status

No Fix - Root caused to a silicon issue that will not be fixed.

Plan Fix - Root caused to a silicon issue and will be fixed in a future stepping.

Fixed - Root caused to a silicon issue and has been fixed in a subsequent stepping.

Spec Change - Root caused to a specification error that will be updated.

Spec Clarification - Root caused to a specification clarification that will be updated.

Spec Clarified - Specification Clarified

Document Change - Root caused to a documentation error that will be updated

Row

Change bar to left of table row indicates that this item is either new or modified from the previous version of this document.

4.2 Errata

Number	Stepping		Status	SKUs (optional)	ERRATA
	C-0	D-1			
1	X	X	No Fix		Northbound merge error seen with three DIMMs per channel
2	X		Fixed		thermal sensor may exhibit response aliasing due to ADC underflow or overflow
3	X	X	No Fix		High current on VTT (0.9V) during certain power sequencing



4.6 Specification Changes

Number	Stepping		SKUs (optional)	SPECIFICATION CHANGE
	C-0	D-1		
1		X		Optional Register Support

5 Errata

1. Northbound merge error seen with three DIMMs per channel

Problem: The roundtrip delay from the next to last Intel® 6400/6402 Advanced Memory Buffer's southbound input to the same AMB's northbound input is smaller than expected when the AMB is in resample mode.

Implication: A northbound merge error may occur.

Workaround: A BIOS workaround was introduced in revision 0.9 of the Memory Reference Code (MRC).

Status: See the Summary Table of Changes for information on steppings affected.

2. Thermal sensor may exhibit response aliasing due to ADC underflow or overflow

Problem: System thermal conditions and the Intel® 6400/6402 Advanced Memory Buffer thermal sensor's thermal slope and accuracy can cause aliasing of the thermal sensor reading.

Implication: The thermal sensor response may indicate high temperature when the actual temperature is very low. Such an event could falsely trigger an overtemperature event if this feature is enabled.

Workaround: None. System developers should not enable the thermal sensor overtemperature feature for affected components.

Status: See the Summary Table of Changes for information on steppings affected.

3. High current on VTT (0.9V) during certain power sequencing

Problem: The Advanced Memory Buffer determines that it is in the S3 mode by checking that VDD (1.8V) is powered up and that VCC (1.5V) is powered off. When in S3, the Advanced Memory Buffer drives all command/address outputs (including CKE, ODT, and CLK) to low. This keeps the DRAM in auto-refresh and helps prevent DRAM data corruption.

Implication: When coming out of S3 mode, if the system brings VTT (0.9V) up before VCC then the AMB will drive low into the VTT pull-up circuitry. Significant current (up to 2x normal) can flow from VTT into the Advanced Memory Buffer during power up or exiting S3. The current in this condition is expected, though the current observed during this brief transition could be 2x the normal current consumption.

Workaround: This current is per DIMM and can be avoided by ensuring VCC is powered up before VTT transitions.

Status: See the Summary Table of Changes for information on steppings affected.



6 Specification Changes

1. Optional Register Support

Issue: Current steppings of the Intel® 6400/6402 Advanced Memory Buffer support registers listed as optional in the *Intel® 6400/6402 Advanced Memory Buffer Datasheet* differently. Steppings after C0 do not support the following optional registers and fields:

Register Name	Function	Offset	Field/Bits
SBFIBPATTBUF2	6	A0h	All
NBFIBPATBUF2	6	E0h	All
SBFIBPATT2EN	6	A4h	All
NBFIBPATT2EN	6	E4h	All
SBMATCHL1	5	C4h	All
SBMATCHL2	5	C8h	All
SBMASKL1	5	D4h	All
SBMASKL2	5	D8h	All
EVENTSEL1	5	E4h	All
EVENTSEL2	5	E8h	All
SBMATCHU	5	BCh	CMD2 [23:16] CMD1 [15:8]
SBMASKU	5	CCh	CMDMASK2 [23:16] CMDMASK1 [15:8]

Affected Docs: *Intel® 6400/6402 Advanced Memory Buffer Datasheet.*

