Intel® X48 Express Chipset

Datasheet

March 2008

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Contents

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Revision History

Revision Number	Description	Revision Date
-001	• Initial Release	March 2008

Intel® 82X48 MCH Features

- Processor/Host Interface (FSB)
  - Supports Intel® Core™2 Duo desktop processor, Intel® Core™2 Quad desktop processor, Intel Core™2 Extreme processor QX9770
  - 800/1067/1333/1600 MT/s (200/266/333/400 MHz) FSB
  - Hyper-Threading Technology (HT Technology)
  - FSB Dynamic Bus Inversion (DBI)
  - 36-bit host bus addressing
  - 12-deep In-Order Queue
  - 1-deep Defer Queue
  - GTL+ bus driver with integrated GTL termination resistors
  - Supports cache Line Size of 64 bytes
- System Memory Interface
  - One or two channels (each channel consisting of 64 data lines)
  - Single or Dual Channel memory organization
  - DDR3-/1333/1066/800 frequencies
  - Intel® Extreme Memory Profile (XMP) DDR memory support at 1600 MHz
  - Unbuffered, non-ECC DDR3 DIMMs
  - Supports 1-Gb, 512-Mb DDR3 technologies for x8 and x16 devices
  - 8 GB maximum memory
- Direct Media Interface (DMI)
  - Chip-to-chip connection interface to Intel ICH9
  - 2 GB/s point-to-point DMI to ICH9 (1 GB/s each direction)
  - 100 MHz reference clock (shared with PCI Express graphics attach)
  - 32-bit downstream addressing
  - Messaging and Error Handling
- PCI Express* Interface
  - Two x16 PCI Express ports
  - Compatible with the *PCI Express Base Specification, Revision 2.0*
  - Raw bit rate on data pins of 5 Gb/s resulting in a real bandwidth per pair of 500 MB/s
- Thermal Sensor
  - Catastrophic Trip Point support
- Power Management
  - PC99 suspend to DRAM support (“STR”, mapped to ACPI state S3)
  - ACPI Revision 2.0 compatible power management
  - Supports processor states: C0 and C1
  - Supports System states: S0, S1, S3 (Cold), and S5
  - Supports processor Thermal Management 2
- Package
  - FC-BGA
  - 40 mm × 40 mm package size
  - 1300 balls, located in a non-grid pattern

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1 Introduction

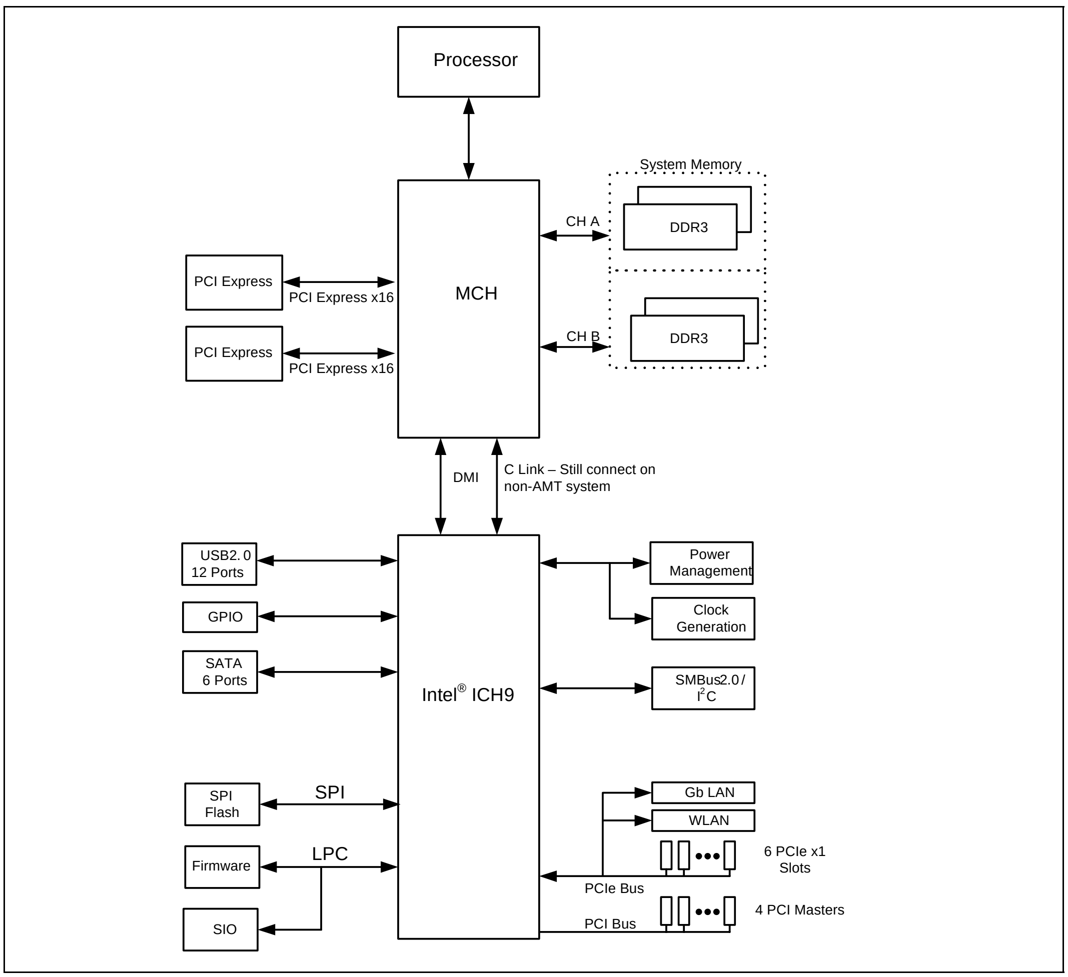
The Intel® X48 Express Chipset is designed for use with the Intel® Core^{TM}2 Duo processors, Intel® Core™2 Quad processors, and Intel Core™2 Extreme processor QX9770 with a 1600 MHz FSB in high-end desktop and workstation platforms. The chipset contains two components: 82X48 MCH for the host bridge and I/O Controller Hub 9 (ICH9) for the I/O subsystem. The ICH9 is the ninth generation I/O Controller Hub and provides a multitude of I/O related functions. Figure 1 shows an example system block diagram for the Intel® X48 Express Chipset.

This document is the datasheet for the Intel® 82X48 Memory Controller Hub (MCH). Topics covered include; signal description, system memory map, PCI register description, a description of the MCH interfaces and major functional units, electrical characteristics, ballout definitions, and package characteristics.

Note: Unless otherwise specified, ICH9 refers to the Intel® 82801IB ICH9 and Intel® 82801IR ICH9R I/O Controller Hub 9 components.

Note: The term ICH9 refers to the ICH9 and ICH9R components.

Figure 1. Intel® X48 Express Chipset System Diagram Example



1.1 Terminology

Term	Description
Chipset / Root – Complex	Used in this specification to refer to one or more hardware components that connect processor complexes to the I/O and memory subsystems. The chipset may include a variety of integrated devices.
CLink	Controller Link is a proprietary chip-to-chip connection between the MCH and ICH. The Intel® X48 Express Chipset requires that Clink is connected in the platform.
Core	The internal base logic in the MCH
CPU	Refers to the processors.
DBI	Dynamic Bus Inversion
DDR3	A third generation Double Data Rate SDRAM memory technology
DMI	Direct Media Interface is a proprietary chip-to-chip connection between the MCH and ICH. This interface is based on the standard PCI Express* specification.
Domain	A collection of physical, logical or virtual resources that are allocated to work together. Domain is used as a generic term for virtual machines, partitions, etc.
EP	PCI Express Egress Port
FSB	Front Side Bus. Synonymous with Host or processor bus
Full Reset	Full reset is when PWROK is de-asserted. Warm reset is when both RSTIN# and PWROK are asserted.
MCH	Memory Controller Hub component that contains the processor interface, DRAM controller, and PCI Express port. It communicates with the I/O controller hub (Intel® ICH9) over the DMI interconnect. Throughout this document, MCH refers to the Intel® X48 Express Chipset MCH, unless otherwise specified.
Host	This term is used synonymously with processor
INTx	An interrupt request signal where X stands for interrupts A, B, C and D
Intel® ICH9	Ninth generation I/O Controller Hub component that contains the primary PCI interface, LPC interface, USB2.0, SATA, and other I/O functions. For this MCH, the term ICH refers to the ICH9.
IOQ	In Order Queue
MSI	Message Signaled Interrupt. A transaction conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
OOQ	Out of Order Queueing
PCI Express*	A high-speed serial interface whose configuration is software compatible with the legacy PCI specifications.
Primary PCI	The physical PCI bus that is driven directly by the Intel® ICH9 component. Communication between Primary PCI and the MCH occurs over DMI. The Primary PCI bus is not PCI Bus 0 from a configuration standpoint.
Rank	A unit of DRAM corresponding to eight x8 SDRAM devices in parallel or four x16 SDRAM devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DIMM.

Term	Description
SCI	System Control Interrupt. Used in ACPI protocol.
SERR	System Error. An indication that an unrecoverable error has occurred on an I/O bus.
SMI	System Management Interrupt. Used to indicate any of several system conditions such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity.
VCO	Voltage Controlled Oscillator

1.2 Reference Documents

Table 1. Intel Specification

Document Name	Location
Intel® X48 Express Chipset Specification Update	http://www.intel.com/design/chipsets/specupdt/319123.htm
Intel® X38 and X48 Express Chipset Thermal and Mechanical Design Guide	http://www.intel.com/design/chipsets/designex/317612.htm
Intel® Core™2 Duo Processor and Intel® Pentium® Dual Core Thermal and Mechanical Design Guide	http://www.intel.com/design/processor/designex/317804.htm
Intel® I/O Controller Hub 9 (ICH9) Family Thermal Mechanical Design Guide.	http://www.intel.com/design/chipsets/designex/316974.htm
Intel® I/O Controller Hub 9 (ICH9) Family Datasheet	http://www.intel.com/design/chipsets/datashts/316972.htm
Intel® X48 Express Chipset Memory Technology and Configuration Guide White Paper	http://www.intel.com/design/chipsets/applnots/319125.htm
Intel® Extreme Memory Profile (Intel® XMP) supporting Intel® X48 Express Chipset with DDR3 White Paper	http://www.intel.com/design/chipsets/applnots/319124.htm
Advanced Configuration and Power Interface Specification, Version 2.0	http://www.acpi.info/
Advanced Configuration and Power Interface Specification, Version 1.0b	http://www.acpi.info/
The PCI Local Bus Specification, Version 2.3	http://www.pcisig.com/specifications
PCI Express Specification, Version 1.1*	http://www.pcisig.com/specifications

1.3 MCH Overview

The role of a MCH in a system is to manage the flow of information between its four interfaces: the processor interface, the System Memory interface, the PCI Express interface, and the I/O Controller through DMI interface. This includes arbitrating between the four interfaces when each initiates transactions. The MCH supports one or two channels of DDR3 SDRAM. It also supports the PCI Express based external device attach. The Intel® X48 Express Chipset platform supports the ninth generation I/O Controller Hub (Intel® ICH9) to provide I/O related features.

1.3.1 Host Interface

The MCH supports a single LGA775 socket processor. The MCH supports a FSB frequency of 800/1066/1333/1600 MHz. Host initiated I/O cycles are decoded to PCI Express, DMI, or the MCH configuration space. Host initiated memory cycles are decoded to PCI Express, DMI or system memory. PCI Express device accesses to non-cacheable system memory are not snooped on the host bus. Memory accesses initiated from PCI Express using PCI semantics and from DMI to system SDRAM will be snooped on the host bus.

Processor/Host Interface (FSB) Details

- Supports the Intel® Core™2 Duo processors, Intel® Core™2 Quad processors, and Intel Core™2 Extreme processor QX9770 with a 1600 MHz FSB
- Supports Front Side Bus (FSB) at the following Frequency Ranges:
  — 800/1066/1333/1600 MT/s
- Supports FSB Dynamic Bus Inversion (DBI)
- Supports 36-bit host bus addressing, allowing the processor to access the entire 64 GB of the host address space.
- Has a 12-deep In-Order Queue to support up to twelve outstanding pipelined address requests on the host bus
- Has a 1-deep Defer Queue
- Uses GTL+ bus driver with integrated GTL termination resistors
- Supports a Cache Line Size of 64 bytes

1.3.2 System Memory Interface

The MCH integrates a system memory DDR3 controller with two, 64-bit wide interfaces. The buffers support SSTL_1.5 (Stub Series Terminated Logic for 1.5V) signal interfaces. The memory controller interface is fully configurable through a set of control registers.

System Memory Interface Details

- Supports memory data transfer rates of 800, 1066, 1333, 1600 MHz for DDR3. The 1600 MHz memory support requires Intel® Extreme Memory Profile (XMP) DDR3-1600 DIMMs.
- Directly supports one or two channels of DDR3 memory with a maximum of two DIMMs per channel. When using DDR3-1600 XMP DIMMs the X48 MCH supports single DIMM per channel where DIMM1 is populated and DIMM0 is not populated
- Supports single and dual channel memory organization modes.
- Supports a data burst length of eight for all memory organization modes.

- I/O Voltage of 1.5 V for DDR3-800, DDR3-1066, and DDR3-1333. DDR3-1600XMP DIMMs use an I/O voltage of 1.9 V.
- Supports non-ECC DDR3 DIMMs.
- Supports maximum memory bandwidth of 12.8GB/s in single-channel mode or 25.6GB/s in dual-channel mode assuming DDR3-1600 XMP DIMMs are used.
- Supports 512-Mb and 1-Gb DDR3 DRAM technologies for x8 and x16 devices.
- Using 512 Mb device technologies, the smallest memory capacity possible is 256 MB, assuming Single Channel Mode with a single x16 single sided un-buffered non-ECC DIMM memory configuration.
- Using 1 Gb device technologies, the largest memory capacity possible is 8 GB, assuming Dual Channel Mode with four x8 double sided un-buffered non-ECC or ECC DIMM memory configurations. Note: The ability to support greater than the largest memory capacity is subject to availability of higher density memory devices.
- Supports up to 32 simultaneous open pages per channel (assuming 4 ranks of 8 bank devices)
- Supports opportunistic refresh scheme
- Supports Partial Writes to memory using Data Mask (DM) signals

1.3.3 Direct Media Interface (DMI)

Direct Media Interface (DMI) is the chip-to-chip connection between the MCH and ICH9. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software transparent permitting current and legacy software to operate normally.

In order to provide for true isochronous transfers and configurable Quality of Service (QoS) transactions, the ICH9 supports two virtual channels on DMI: VC0 and VC1. These two channels provide a fixed arbitration scheme where VC1 is always the highest priority. VC0 is the default conduit of traffic for DMI and is always enabled. VC1 must be specifically enabled and configured at both ends of the DMI link (i.e., the ICH9 and MCH).

- A chip-to-chip connection interface to Intel ICH9
- 2 GB/s point-to-point DMI to ICH9 (1 GB/s each direction)
- 100 MHz reference clock (shared with PCI Express)
- 32-bit downstream addressing
- APIC and MSI interrupt messaging support. Will send Intel-defined “End Of Interrupt” broadcast message when initiated by the processor.
- Message Signaled Interrupt (MSI) messages
- SMI, SCI, and SERR error indication

1.3.4 PCI Express* Interface

PCI Express* Interface

The MCH supports two 16-lane (x16) PCI Express ports. The PCI Express ports are compliant to the *PCI Express* Base Specification* revision 2.0. The x16 ports operate at a frequency of 5 Gb/s on each lane while employing 8b/10b encoding, and support a maximum theoretical bandwidth of 8.0 GB/s in each direction.

- For the Intel® X48 Express Chipset, two 16-lane PCI Express ports intended for external device attach are supported and compatible to the *PCI Express* Base Specification* revision 2.0.
- PCI Express frequency of 2.5 GHz resulting in 5.0 Gb/s each direction per lane.
- Raw bit-rate on the data pins of 5.0 Gb/s, resulting in a real bandwidth per pair of 500 MB/s given the 8b/10b encoding used to transmit data across this interface
- Maximum theoretical realized bandwidth on the interface of 8 GB/s in each direction simultaneously, for an aggregate of 16 GB/s when x16.
- PCI Express Enhanced Addressing Mechanism allows for accessing the device configuration space in a flat memory mapped fashion.
- Automatic discovery, negotiation, and training of link out of reset.
- Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)
- Supports traditional AGP style traffic (asynchronous non-snooped, PCI Express-relaxed ordering)
- Hierarchical PCI-compliant configuration mechanism for downstream devices (i.e., normal PCI 2.3 Configuration space as a PCI-to-PCI bridge).
- Supports “static” lane numbering reversal. This method of lane reversal is controlled by a Hardware Reset strap, and reverses both the receivers and transmitters for all lanes (e.g., TX[15]->TX[0], RX[15]->RX[0]). This method is transparent to all external devices and is different than lane reversal as defined in the PCI Express Specification. In particular, link initialization is not affected by static lane reversal.
- When two, 16-lane PCI Express ports are used, the second port will support either PCI Express Gen1.1 I/O cards with x8, x4 or x1 lanes or PCI Express Gen1/Gen2 Graphics cards with x16 or x1 lanes.

1.3.5 MCH Clocking

- Differential host clock of 200/266/333/400 MHz. Supports FSB transfer rates of 800/1066/1333/1600 MT/s.
- Differential memory clocks of 400/533/667/800 MHz. Supports memory transfer rates of DDR3-800, DDR3-1067, DDR3-1333, and DDR3-1600 (Intel® XMP memory).
- The PCI Express* PLL of 100 MHz Serial Reference Clock generates the PCI Express core clock of 250 MHz.
- All of the above clocks are capable of tolerating Spread Spectrum clocking.
- Host, memory, and PCI Express PLLs are disabled until PWROK is asserted.

1.3.6 Power Management

MCH Power Management support includes:

- PC99 suspend to DRAM support (“STR”, mapped to ACPI state S3)
- SMRAM space remapping to A0000h (128 KB)
- Supports extended SMRAM space above 256 MB, and cacheable (cacheability controlled by processor)
- ACPI Rev 1.0b compatible power management
- Supports processor states: C0 and C1
- Supports System states: S0, S1, S3(Cold), and S5
- Supports processor Thermal Management 2 (TM2)

1.3.7 Thermal Sensor

The MCH Thermal Sensor support includes:

- Catastrophic Trip Point support for emergency clock gating for the MCH

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2 Signal Description

This section provides a detailed description of MCH signals. The signals are arranged in functional groups according to their associated interface.

The following notations are used to describe the signal type.

Signal Type	Description
PCI Express*	PCI Express interface signals. These signals are compatible with PCI Express 2.0 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ – D-|) * 2 = 1.2 Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
DMI	Direct Media Interface signals. These signals are compatible with PCI Express 1.1 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ – D-|) * 2 = 1.2 Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
CMOS	CMOS buffers. 1.5 V tolerant.
COD	CMOS Open Drain buffers. 3.3 V tolerant.
HVCMOS	High Voltage CMOS buffers. 3.3 V tolerant.
HVIN	High Voltage CMOS input-only buffers. 3.3 V tolerant.
SSTL_1.5	Stub Series Termination Logic. These are 1.5 V output capable buffers. 1.5 V tolerant. DDR3-1600 XMP DIMMs buffers will operate at 1.9 V which is within the SSTL_1.5 tolerances.
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation.
GTL+	Gunning Transceiver Logic signaling technology. Implements a voltage level as defined by V_{TT} of 1.2 V and/or 1.1 V.

2.1 Host Interface Signals

Note: Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the Host Bus (V_{TT}).

Signal Name	Type	Description
FSB_ADSB	I/O GTL+	**Address Strobe:** The processor bus owner asserts FSB_ADSB to indicate the first of two cycles of a request phase. The MCH can assert this signal for snoop cycles and interrupt messages.
FSB_BNRB	I/O GTL+	**Block Next Request:** Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
FSB_BPRIB	O GTL+	**Priority Agent Bus Request:** The MCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the FSB_LOCKB signal was asserted.
FSB_BREQ0B	O GTL+	**Bus Request 0:** The MCH pulls the processor bus' FSB_BREQ0B signal low during FSB_CPURSTB. The processors sample this signal on the active-to-inactive transition of FSB_CPURSTB. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 HCLKs and the maximum hold time is 20 HCLKs. FSB_BREQ0B should be tristated after the hold time requirement has been satisfied.
FSB_CPURSTB	O GTL+	**CPU Reset:** The FSB_CPURSTB pin is an output from the MCH. The MCH asserts FSB_CPURSTB while RSTINB (PCIRST# from the ICH) is asserted and for approximately 1 ms after RSTINB is de-asserted. The FSB_CPURSTB allows the processors to begin execution in a known state.
FSB_DBSYB	I/O GTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
FSB_DEFERB	O GTL+	**Defer:** Signals that the MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
FSB_DINVB_[3:0]	I/O GTL+ 4x	**Dynamic Bus Inversion:** Driven along with the FSB_DB_[63:0] signals. Indicates if the associated signals are inverted or not. FSB_DINVB_[3:0] are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16 bit group never exceeds 8. **FSB_DINVB_x** — **Data Bits** FSB_DINVB_3 — FSB_DB_[63:48] FSB_DINVB_2 — FSB_DB_[47:32] FSB_DINVB_1 — FSB_DB_[31:16] FSB_DINVB_0 — FSB_DB_[15:0]
FSB_DRDYB	I/O GTL+	**Data Ready:** Asserted for each cycle that data is transferred.

Signal Name	Type	Description
FSB_AB_[35:3]	I/O GTL+ 2x	**Host Address Bus:** FSB_AB_[35:3] connect to the processor address bus. During processor cycles the FSB_AB_[35:3] are inputs. The MCH drives FSB_AB_[35:3] during snoop cycles on behalf of DMI and PCI Express initiators. FSB_AB_[35:3] are transferred at 2x rate. Note that the address is inverted on the processor bus. The values are driven by the MCH between PWROK assertion and FSB_CPURSTINB de-assertion to allow processor configuration.
FSB_ADSTBB_[1:0]	I/O GTL+ 2x	**Host Address Strobe:** The source synchronous strobes used to transfer FSB_AB_[31:3] and FSB_REQB_[4:0] at the 2x transfer rate. **Strobe** — **Address Bits** FSB_ADSTBB_0 — FSB_AB_[16:3], FSB_REQB_[4:0] FSB_ADSTBB_1 — FSB_AB_[31:17]
FSB_DB_[63:0]	I/O GTL+ 4x	**Host Data:** These signals are connected to the processor data bus. Data on FSB_DB_[63:0] is transferred at a 4x rate. Note that the data signals may be inverted on the processor bus, depending on the FSB_DINVB_[3:0] signals.
FSB_DSTBPB_[3:0] FSB_DSTBNB_[3:0]	I/O GTL+ 4x	**Differential Host Data Strobes:** The differential source synchronous strobes used to transfer FSB_DB_[63:0] and FSB_DINVB_[3:0] at the 4x transfer rate. Named this way because they are not level sensitive. Data is captured on the falling edge of both strobes. Hence, they are pseudo-differential, and not true differential. **Strobe** — **Data Bits** FSB_DSTB[P,N]B_3 — FSB_DB_[63:48], HDINVB_3 FSB_DSTB[P,N]B_2 — FSB_DB_[47:32], HDINVB_2 FSB_DSTB[P,N]B_1 — FSB_DB_[31:16], HDINVB_1 FSB_DSTB[P,N]B_0 — FSB_DB_[15:0], HDINVB_0
FSB_HITB	I/O GTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with FSB_HITMB by the target to extend the snoop window.
FSB_HITMB	I/O GTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with FSB_HITB to extend the snoop window.
FSB_LOCKB	I GTL+	**Host Lock:** All processor bus cycles sampled with the assertion of FSB_LOCKB and FSB_ADSB, until the negation of FSB_LOCKB must be atomic (i.e. *no DMI or PCI Express access* to DRAM are allowed when FSB_LOCKB is asserted by the processor).
FSB_REQB_[4:0]	I/O GTL+ 2x	**Host Request Command:** Defines the attributes of the request. FSB_REQB_[4:0] are transferred at 2x rate. Asserted by the requesting agent during both halves of Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type. The transactions supported by the MCH Host Bridge are defined in the Host Interface section of this document.

Signal Name	Type	Description
FSB_TRDYB	O GTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.
FSB_RSB_[2:0]	O GTL+	**Response Signals:** Indicates type of response according to the table at left: **Encoding** **Response Type** 000 Idle state 001 Retry response 010 Deferred response 011 *Reserved (not driven by* MCH*)* 100 *Hard Failure (not driven by* MCH*)* 101 No data response 110 Implicit Writeback 111 Normal data response
FSB_RCOMP	I/O A	**Host RCOMP:** Used to calibrate the Host GTL+ I/O buffers. This signal is powered by the Host Interface termination rail (V_{TT}). Connects to FSB_XRCOMP1IN in the package.
FSB_SCOMP	I/O A	**Slew Rate Compensation:** Compensation for the Host Interface for rising edges.
FSB_SCOMPB	I/O A	**Slew Rate Compensation:** Compensation for the Host Interface for falling edges.
FSB_SWING	I/O A	**Host Voltage Swing:** These signals provide reference voltages used by the FSB RCOMP circuits. FSB_XSWING is used for the signals handled by FSB_XRCOMP.
FSB_DVREF	I/O A	**Host Reference Voltage:** Reference voltage input for the Data signals of the Host GTL interface.
FSB_ACCVREF	I/O A	**Host Reference Voltage:** Reference voltage input for the Address signals of the Host GTL interface.

2.2 System Memory (DDR3) Interface Signals

2.2.1 System Memory Channel A Interface Signals

Signal Name	Type	Description
DDR_A_CK	O SSTL-1.5	**SDRAM Differential Clocks:** — DDR3: Two per DIMM
DDR_A_CKB	O SSTL-1.5	**SDRAM Inverted Differential Clocks:** — DDR3: Two per DIMM
DDR_A_CSB_3 DDR_A_CSB_2 DDR_A_CSB_0	O SSTL-1.5	**DDR3 Device Rank 3, 2, and 0 Chip Selects**
DDR3_A_CSB_1	O SSTL-1.5	**DDR3 Device Rank 1 Chip Select**
DDR_A_CKE_[3:0]	O SSTL-1.5	**DDR3 Clock Enable:** (1 per Device Rank)
DDR_A_ODT_[3:0]	O SSTL-1.5	**DDR3 On Die Termination:** (1 per Device Rank)
DDR_A_MA_[14:1]	O SSTL-1.5	**DDR3 Address Signals [14:1]**
DDR3_A_MA_0	O SSTL-1.5	**DDR3 Address Signal 0**
DDR_A_BS_[2:0]	O SSTL-1.5	**DDR3 Bank Select**
DDR_A_RASB	O SSTL-1.5	**DDR3 Row Address Select signal**
DDR_A_CASB	O SSTL-1.5	**DDR3 Column Address Select signal**
DDR3_A_WEB	O SSTL-1.5	**DDR3 Write Enable signal**
DDR_A_DQ_[63:0]	I/O SSTL-1.5	**DDR3 Data Lines**
DDR_A_DM_[7:0]	O SSTL-1.5	**DDR3 Data Mask**
DDR_A_DQS_[8:0]	I/O SSTL-1.5	**DDR3 Data Strobes**
DDR_A_DQSB_[8:0]	I/O SSTL-1.5	**DDR3 Data Strobe Complements**

2.2.2 System Memory Channel B Interface Signals

Signal Name	Type	Description
DDR_B_CK	O SSTL-1.5	**SDRAM Differential Clocks:** — DDR3: Two per DIMM
DDR_B_CKB	O SSTL-1.5	**SDRAM Inverted Differential Clocks:** — DDR3: Two per DIMM
DDR_B_CSB_[3:0]	O SSTL-1.5	**DDR3 Device Rank 3, 2, 1, and 0 Chip Select**
DDR_B_CKE_[3:0]	O SSTL-1.5	**DDR3 Clock Enable:** (1 per Device Rank)
DDR_B_ODT_[2:0]	O SSTL-1.5	**DDR3 Device Rank 2, 1, and 0 On Die Termination**
DDR3_B_ODT_3	O SSTL-1.5	**DDR3 Device Rank 3 On Die Termination**
DDR_B_MA_[14:0]	O SSTL-1.5	**DDR3 Address Signals [14:0]**
DDR_B_BS_[2:0]	O SSTL-1.5	**DDR3 Bank Select**
DDR_B_RASB	O SSTL-1.5	**DDR3 Row Address Select signal**
DDR_B_CASB	O SSTL-1.5	**DDR3 Column Address Select signal**
DDR_B_WEB	O SSTL-1.5	**DDR3 Write Enable signal**
DDR_B_DQ_[63:0]	I/O SSTL-1.5	**DDR3 Data Lines**
DDR_B_DM_[7:0]	O SSTL-1.5	**DDR3 Data Mask**
DDR_B_DQS_[8:0]	I/O SSTL-1.5	**DDR3 Data Strobes**
DDR_B_DQSB_[8:0]	I/O SSTL-1.5	**DDR3 Data Strobe Complements**

2.2.3 System Memory Miscellaneous Signals

Signal Name	Type	Description
DDR_RCOMPXPD	I/O A	**System Memory Pull-down RCOMP**
DDR_RCOMPXPU	I/O A	**System Memory Pull-up RCOMP**
DDR_RCOMPYPD	I/O A	**System Memory Pull-down RCOMP**
DDR_RCOMPYPU	I/O A	**System Memory Pull-up RCOMP**
DDR_VREF	I A	**System Memory Reference Voltage**
DDR_RCOMPVOH	I A	**System Memory Pull-up Reference Signal**
DDR_RCOMPVOL	I A	**System Memory Pull-down Reference Signal**
DDR3_DRAM_PWROK	I A	**DDR3 VCC_DDR Power OK**
DDR3_DRAMRSTB	O SSTL-1.5	**DDR3 Reset Signal**

2.3 PCI Express* Interface Signals

Signal Name	Type	Description
PEG_RXN_[15:0] PEG_RXP_[15:0]	I/O PCIE	**Primary PCI Express Receive Differential Pair.** The MCH supports a maximum width of x16 where all lanes are used.
PEG_TXN_[15:0] PEG_TXP_[15:0]	O PCIE	**Primary PCI Express Transmit Differential Pair.** The MCH supports a maximum width of x16 where all lanes are used.
PEG2_RXN_[15:0] PEG2_RXP_[15:0]	I/O PCIE	**Secondary PCI Express Receive Differential Pair.** The MCH supports a maximum width of x16 where all lanes are used.
PEG2_TXN_[15:0] PEG2_TXP_[15:0]	O PCIE	**Secondary PCI Express Transmit Differential Pair.** The MCH supports a maximum width of x16 where all lanes are used.
EXP_COMPO	I A	**Primary PCI Express Output Current Compensation**
EXP_COMPI	I A	**Primary PCI Express Input Current Compensation**
EXP2_COMPO	I A	**Secondary PCI Express Output Current Compensation**
EXP2_COMPI	I A	**Secondary PCI Express Input Current Compensation**

2.4 Controller Link Interface Signals

Signal Name	Type	Description
CL_DATA	I/O CMOS	**Controller Link Data (Bi-directional)**
CL_CLK	I/O CMOS	**Controller Link Clock (Bi-directional)**
CL_VREF	I CMOS	**Controller Link VREF**
CL_RST#	I CMOS	**Controller Link Reset (Active low)**

2.5 Clocks, Reset, and Miscellaneous

Signal Name	Type	Description
HPL_CLKINP HPL_CLKINN	I CMOS	**Differential Host Clock In:** These pins receive a differential host clock from the external clock synthesizer. This clock is used by all of the MCH logic that is in the Host clock domain.
EXP_CLKINP EXP_CLKINN	I CMOS	**Differential Primary PCI Express Clock In:** These pins receive a differential 100 MHZ Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of Primary PCI Express and DMI.
EXP2_CLKINP EXP2_CLKINN	I CMOS	**Differential Secondary PCI Express Clock In:** These pins receive a differential 100 MHZ Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of Secondary PCI Express.
RSTINB	I SSTL	**Reset In:** When asserted this signal will asynchronously reset the MCH logic. This signal is connected to the PCIRST# output of the ICH. All PCI Express output signals and DMI output signals will also tri-state compliant to PCI Express Rev 2.0 specification. This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3 V tolerant.
CL_PWROK	I/O SSTL	**CL Power OK:** When asserted, CL_PWROK is an indication to the MCH that core power (VCC_CL) has been stable for at least 10us.
EXP_SLR	I CMOS	**PCI Express* Static Lane Reversal/Form Factor Selection:** MCH's PCI Express lane numbers are reversed to differentiate BTX and ATX form factors 0 = MCH PCI Express lane numbers are reversed (BTX) 1 = Normal operation (ATX)

Signal Name	Type	Description
BSEL[2:0]	I CMOS	**Bus Speed Select:** At the de-assertion of PWROK, the value sampled on these pins determines the expected frequency of the bus.
MTYPE	I GTL+	**Memory Type:** This pin determines memory support. 0 = DDR3 1 = N/A
PWROK	I/O SSTL	**Power OK:** When asserted, PWROK is an indication to the MCH that core power has been stable for at least 10 us.
ICH_SYNCB	O HVCMOS	**ICH Sync:** This signal synchronizes the MCH with the ICH.
ALLZTEST	I GTL+	**All Z Test:** Used for Chipset Bed of Nails testing to execute All Z Test. It is used as output for XOR Chain testing.
XORTEST	I GTL+	**XOR Chain Test:** Used for Chipset Bed of Nails testing to execute XOR Chain Test.
TEST[3:0]	I/O A	**In Circuit Test:** These pins should be connected to test points on the motherboard. They are internally shorted to the package ground and can be used to determine if the corner balls on the MCH are correctly soldered down to the motherboard. These pins should NOT connect to ground on the motherboard. If TEST[3:0] are not going to be used, they should be left as no connects.

2.6 Direct Media Interface

Signal Name	Type	Description
DMI_RXP_[3:0] DMI_RXN_[3:0]	I DMI	**Direct Media Interface:** Receive differential pair (RX). MCH-ICH serial interface input
DMI_TXP_[3:0] DMI_TXN_[3:0]	O DMI	**Direct Media Interface:** Transmit differential pair (TX). MCH-ICH serial interface output

2.7 Power and Grounds

Name	Voltage	Description
VCC	1.25 V	**Core Power**
VTT	1.1 V/1.2 V	**Processor System Bus Power**
VCC_EXP	1.25 V	**PCI Express* and DMI Power**
VCC_DDR	1.5V[1]	**DDR3 System Memory Power**
VCC_CKDDR	1.5V[1]	**DDR3 System Clock Memory Power**
VCC3_3	3.3 V	**3.3 V CMOS Power**
VCCAPLL_EXP	1.25 V	**Primary PCI Express PLL Analog Power**
VCCAPLL_EXP2	1.25 V	**Secondary PCI Express PLL Analog Power**
VCCA_hplL	1.25 V	**Host PLL Analog Power**
VCCA_mpl	1.25 V	**System Memory PLL Analog Power**
VCCABG_EXP	3.3 V	**PCI Express* Analog Power**
VCC_CL	1.25 V	**Controller Link Aux Power**
VSS	0 V	**Ground**

NOTES:
1. DDR3-800, DDR3-1066, and DDR3-1333 DIMMs require 1.5 V derived from the boards VCCSM power rail. DDR3-1600 XMP DIMMs require 1.9 V.

§ §§

3 System Address Map

The MCH supports 64 GB (36 bit) of host address space and 64 KB+3 of addressable I/O space. There is a programmable memory address space under the 1 MB region which is divided into regions which can be individually controlled with programmable attributes such as Disable, Read/Write, Write Only, or Read Only. Attribute programming is described in the Register Description section. This section focuses on how the memory space is partitioned and what the separate memory regions are used for. I/O address space has simpler mapping and is explained near the end of this section.

The MCH supports PCI Express* upper pre-fetchable base/limit registers. This allows the PCI Express unit to claim I/O accesses above 36 bit, complying with the PCI Express Specification. Addressing of greater than 8 GB is allowed on either the DMI Interface or PCI Express interface. The MCH supports a maximum of 8 GB of DRAM. No DRAM memory will be accessible above 8 GB.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI Interface. The MCH does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable DRAM). The TOLUD register is set to the appropriate value by BIOS. The reclaim base/reclaim limit registers remap logical accesses bound for addresses above 4 GB onto physical addresses that fall within DRAM.

The Address Map includes a number of programmable ranges:

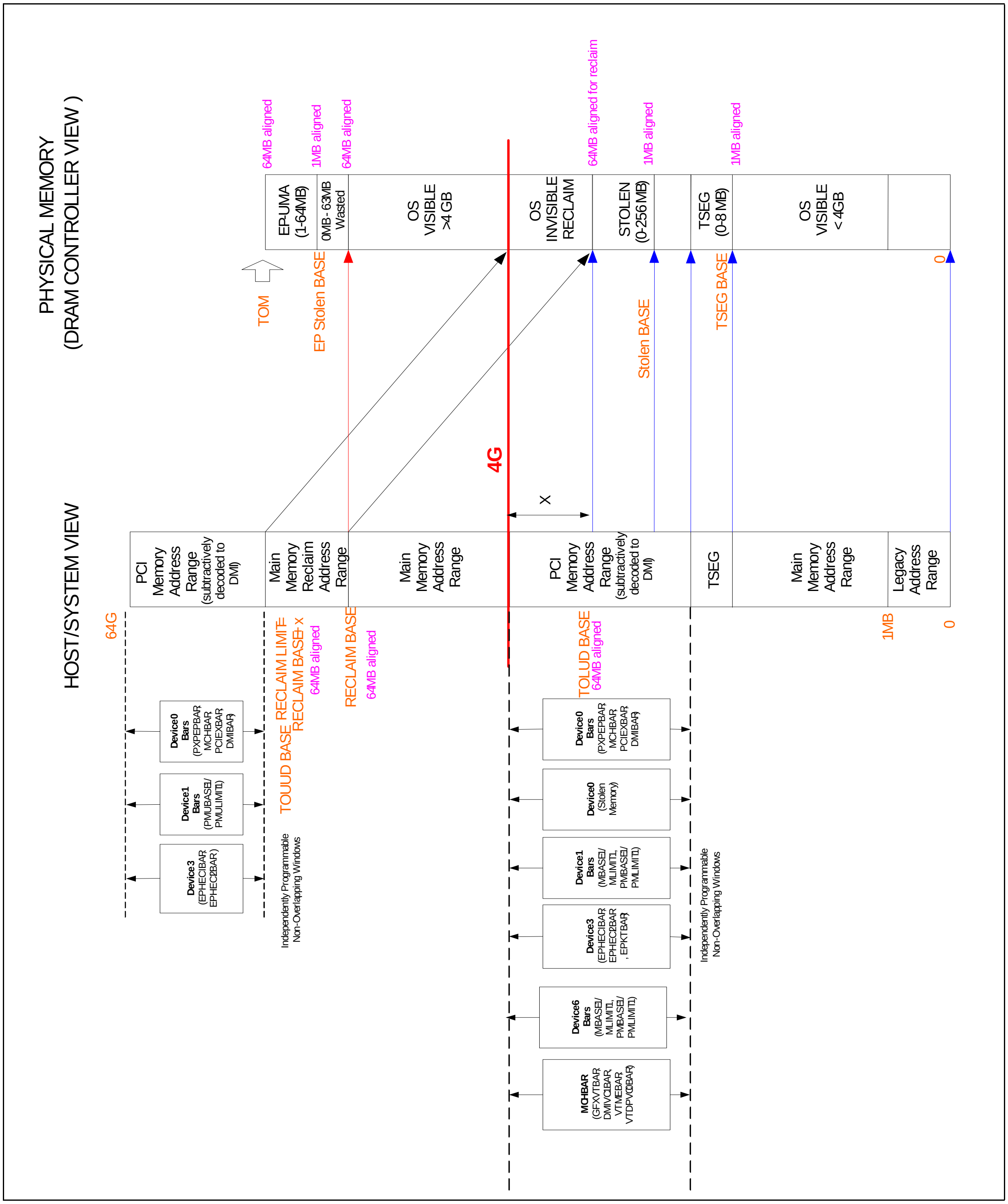
- Device 0
  - PXPEPBAR – Egress port registers. Necessary for setting up VC1 as an isochronous channel using time based weighted round robin arbitration. (4 KB window)
  - MCHBAR – Memory mapped range for internal MCH registers. For example, memory buffer register controls. (16 KB window)
  - PCIEXBAR – Flat memory-mapped address spaced to access device configuration registers. This mechanism can be used to access PCI configuration space (0–FFh) and Extended configuration space (100h–FFFh) for PCI Express devices. This enhanced configuration access mechanism is defined in the PCI Express specification. (64 MB, 128 MB, or 256 MB window).
  - DMIBAR –This window is used to access registers associated with the Direct Media Interface (DMI) register memory range. (4 KB window)
- Device 1
  - MBASE1/MLIMIT1 – PCI Express port non-prefetchable memory access window.
  - PMBASE1/PMLIMIT1 – PCI Express port prefetchable memory access window.
  - PMUBASE/PMULIMIT – PCI Express port upper prefetchable memory access window
  - IOBASE1/IOLIMIT1 – PCI Express port I/O access window.
- Device 6, Function 0
  - MBASE1/MLIMIT1 – PCI Express port non-prefetchable memory access window.
  - PMBASE1/PMLIMIT1 – PCI Express port prefetchable memory access window.
  - PMUBASE/PMULIMIT – PCI Express port upper prefetchable memory access window
  - IOBASE1/IOLIMIT1 – PCI Express port I/O access window.

The rules for the above programmable ranges are:

1. ALL of these ranges MUST be unique and NON-OVERLAPPING. It is the BIOS or system designers' responsibility to limit memory population so that adequate PCI, PCI Express, High BIOS, and PCI Express Memory Mapped space, and APIC memory space can be allocated.
2. In the case of overlapping ranges with memory, the memory decode will be given priority.
3. There are NO Hardware Interlocks to prevent problems in the case of overlapping ranges.
4. Accesses to overlapped ranges may produce indeterminate results.
5. The only peer-to-peer cycles allowed below the top of Low Usable memory (register TOLUD) are DMI Interface to PCI Express range writes.

Figure 2 represents system memory address map in a simplified form.

Figure 2. MCH System Address Ranges



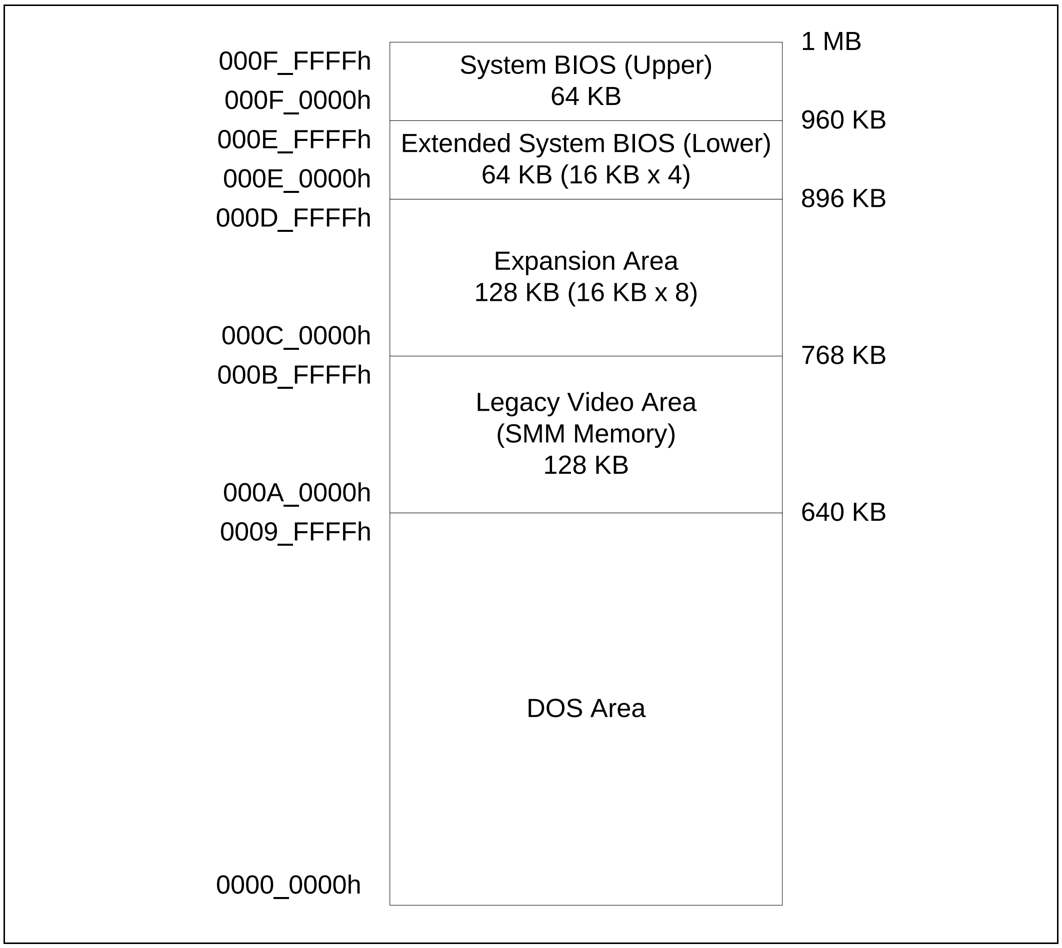
NOTE: For non-AMT system such as Intel® X48 chipset platforms, do not follow the EP UMA requirement.

3.1 Legacy Address Range

This area is divided into the following address regions:

- 0 - 640 KB – DOS Area
- 640 - 768 KB – Legacy Video Buffer Area
- 768 - 896 KB in 16 KB sections (total of 8 sections) – Expansion Area
- 896 -960 KB in 16 KB sections (total of 4 sections) – Extended System BIOS Area
- 960 KB - 1 MB Memory – System BIOS Area

Figure 3. DOS Legacy Address Range



3.1.1 DOS Range (0h – 9_FFFFh)

The DOS area is 640 KB (0000_0000h – 0009_FFFFh) in size and is always mapped to the main memory controlled by the MCH.

3.1.2 Expansion Area (C_0000h-D_FFFFh)

This 128 KB ISA Expansion region (000C_0000h – 000D_FFFFh) is divided into eight 16 KB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through MCH and are subtractive decoded to ISA space. Memory that is disabled is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 2. Expansion Area Memory Segments

Memory Segments	Attributes	Comments
0C0000h – 0C3FFFh	WE RE	Add-on BIOS
0C4000h – 0C7FFFh	WE RE	Add-on BIOS
0C8000h – 0CBFFFh	WE RE	Add-on BIOS
0CC000h – 0CFFFFh	WE RE	Add-on BIOS
0D0000h – 0D3FFFh	WE RE	Add-on BIOS
0D4000h – 0D7FFFh	WE RE	Add-on BIOS
0D8000h – 0DBFFFh	WE RE	Add-on BIOS
0DC000h – 0DFFFFh	WE RE	Add-on BIOS

3.1.3 Extended System BIOS Area (E_0000h–E_FFFFh)

This 64 KB area (000E_0000h – 000E_FFFFh) is divided into four 16 KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to DMI Interface. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 3. Extended System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0E0000h – 0E3FFFh	WE RE	BIOS Extension
0E4000h – 0E7FFFh	WE RE	BIOS Extension
0E8000h – 0EBFFFh	WE RE	BIOS Extension
0EC000h – 0EFFFFh	WE RE	BIOS Extension

3.1.4 System BIOS Area (F_0000h–F_FFFFh)

This area is a single 64 KB segment (000F_0000h – 000F_FFFFh). This segment can be assigned read and write attributes. It is by default (after reset) Read/Write disabled and cycles are forwarded to DMI Interface. By manipulating the Read/Write attributes, the MCH can “shadow” BIOS into the main DRAM. When disabled, this segment is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 4. System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0F0000h – 0FFFFFh	WE RE	BIOS Area

3.1.5 PAM Memory Area Details

The 13 sections from 768 KB to 1 MB comprise what is also known as the PAM Memory Area.

The MCH does not handle IWB (Implicit Write-Back) cycles targeting DMI. Since all memory residing on DMI should be set as non-cacheable, there will normally not be IWB cycles targeting DMI. However, DMI becomes the default target for processor and DMI originated accesses to disabled segments of the PAM region. If the MTRRs covering the PAM regions are set to WB or RD it is possible to get IWB cycles targeting DMI. This may occur for processor originated cycles (in a DP system) and for DMI originated cycles to disabled PAM regions.

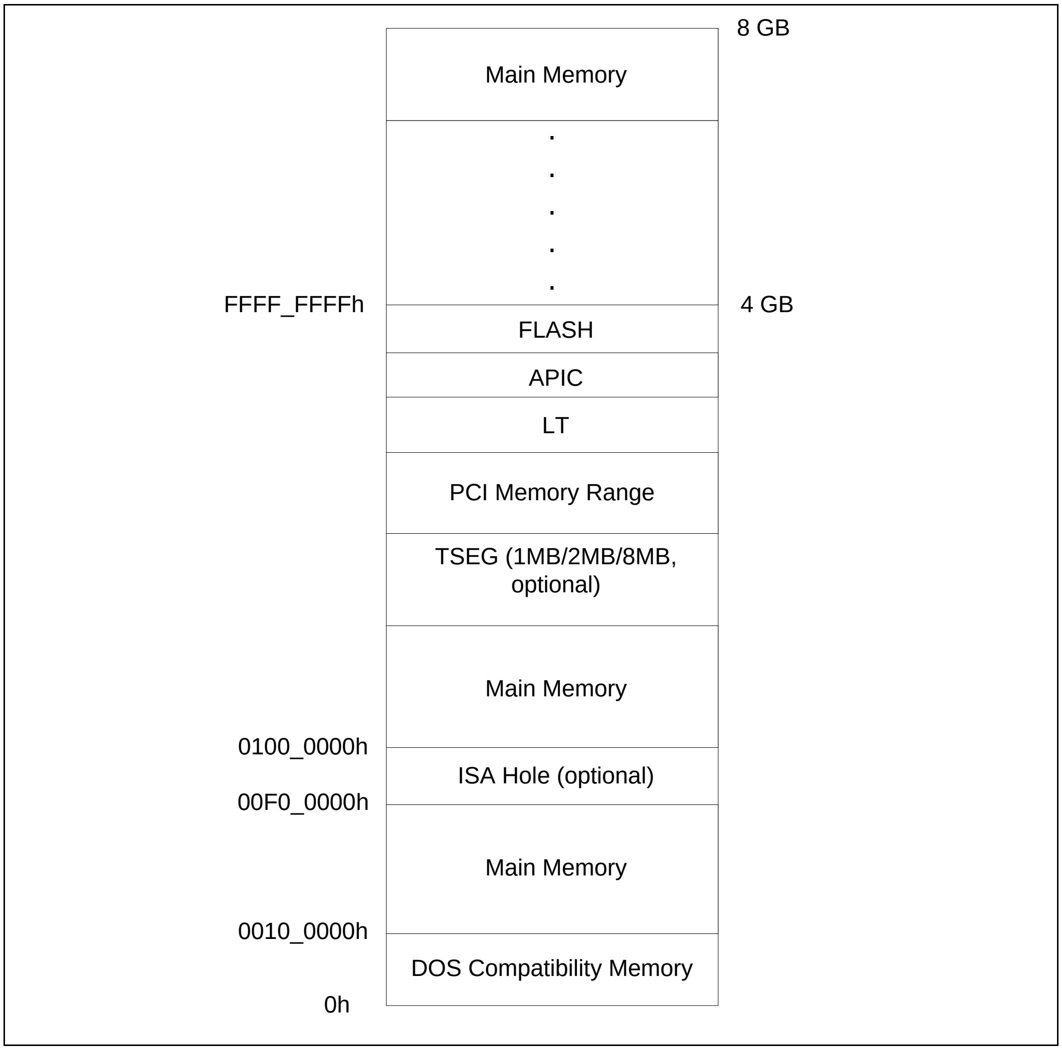
For example, say that a particular PAM region is set for “Read Disabled” and the MTRR associated with this region is set to WB. A DMI master generates a memory read targeting the PAM region. A snoop is generated on the FSB and the result is an IWB. Since the PAM region is “Read Disabled” the default target for the Memory Read becomes DMI. The IWB associated with this cycle will cause the MCH to hang.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

3.2 Main Memory Address Range (1MB - TOLUD)

This address range extends from 1 MB to the top of Low Usable physical memory that is permitted to be accessible by the MCH (as programmed in the TOLUD register). All accesses to addresses within this range will be forwarded by the MCH to the DRAM unless it falls into the optional TSEG, or optional ISA Hole.

Figure 4. Main Memory Address Range



3.2.1 ISA Hole (15 MB –16 MB)

A hole can be created at 15 MB –16 MB as controlled by the fixed hole enable in Device 0 space. Accesses within this hole are forwarded to the DMI Interface. The range of physical DRAM memory disabled by opening the hole is not remapped to the top of the memory – that physical DRAM space is not accessible. This 15 MB – 16 MB hole is an optionally enabled ISA hole.

The ISA Hole is used by validation and customer SV teams for some of their test cards. That is why it is being supported. There is no inherent BIOS request for the 15 – 16 MB window.

3.2.2 TSEG

TSEG is optionally 1 MB, 2 MB, or 8 MB in size. TSEG is below stolen memory, which is at the top of Low Usable physical memory (TOLUD). SMM-mode processor accesses to enabled TSEG access the physical DRAM at the same address. Non-processor originated accesses are not allowed to SMM space. PCI Express, and DMI originated cycles to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, processor accesses to the TSEG range without a SMM attribute or without WB attribute are also forwarded to memory as invalid accesses. Non-SMM-mode Write Back cycles that target TSEG space are completed to DRAM for cache coherency. When SMM is enabled the maximum amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register which is fixed at 1 MB, 2 MB, or 8 MB.

3.2.3 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOLUD) are created for SMM-mode, and stolen memory. **It is the responsibility of BIOS to properly initialize these regions.** Table 7 details the location and attributes of the regions.

Table 5. Pre-allocated Memory Example for 64 MB DRAM, 1 MB stolen and 1 MB TSEG

Memory Segments	Attributes	Comments
0000_0000h – 03CF_FFFFh	R/W	Available System Memory 61 MB
03D0_0000h – 03DF_FFFFh	SMM Mode Only - processor Reads	TSEG Address Range & Pre-allocated Memory

3.3 PCI Memory Address Range (TOLUD – 4GB)

This address range, from the top of low usable DRAM (TOLUD) to 4 GB is normally mapped to the DMI Interface.

Device 0 exceptions are:

- Addresses decoded to the egress port registers (PXPEPBAR)
- Addresses decoded to the memory mapped range for internal MCH registers (MCHBAR)
- Addresses decoded to the flat memory-mapped address spaced to access device configuration registers (PCIEXBAR)
- Addresses decoded to the registers associated with the Direct Media Interface (DMI) register memory range. (DMIBAR)

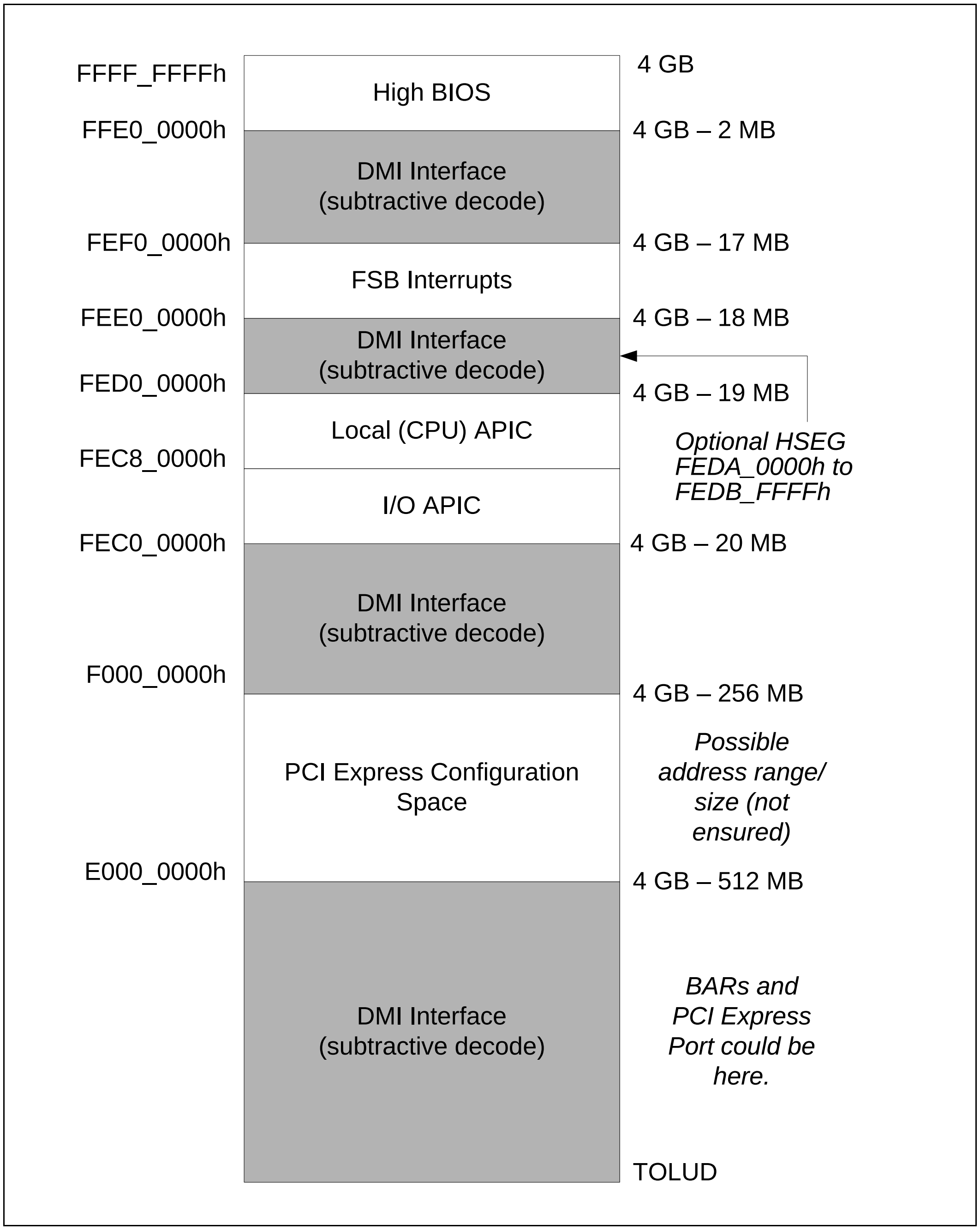
With PCI Express port, there are two exceptions to this rule.

- Addresses decoded to the PCI Express Memory Window defined by the MBASE1, MLIMIT1, registers are mapped to PCI Express.
- Addresses decoded to the PCI Express prefetchable Memory Window defined by the PMBASE1, PMLIMIT1, registers are mapped to PCI Express.

Some of the MMIO Bars may be mapped to this range or to the range above TOUUD.

There are sub-ranges within the PCI Memory address range defined as APIC Configuration Space, FSB Interrupt Space, and High BIOS Address Range. The exceptions listed above for the PCI Express ports ***MUST NOT*** *overlap with these ranges.*

Figure 5. PCI Memory Address Range



3.3.1 APIC Configuration Space (FEC0_0000h – FECF_FFFFh)

This range is reserved for APIC configuration space. The I/O APIC(s) usually reside in the ICH portion of the chip-set.

The IOAPIC spaces are used to communicate with IOAPIC interrupt controllers that may be populated in the system. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. Processor accesses to the default IOAPIC region (FEC0_0000h to FEC7_FFFFh) are always forwarded to DMI.

The MCH optionally supports additional I/O APICs behind the PCI Express port. When enabled via the PCI Express Configuration register (Device 1 Offset 200h), the PCI Express port will positively decode a subset of the APIC configuration space – specifically FEC8_0000h thru FECF_FFFFh. Memory request to this range would then be forwarded to the PCI Express port. When disabled, any access within entire APIC Configuration space (FEC0_0000h to FECF_FFFFh) is forwarded to DMI.

3.3.2 HSEG (FEDA_0000h – FEDB_FFFFh)

This optional segment from FEDA_0000h to FEDB_FFFFh provides a remapping window to SMM Memory. It is sometimes called the High SMM memory space. SMM-mode processor accesses to the optionally enabled HSEG are remapped to 000A_0000h – 000B_FFFFh. Non-SMM-mode processor accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode Write Back cycles which are remapped to SMM space to maintain cache coherency. PCI Express and DMI originated cycles to enabled SMM space are not allowed. Physical DRAM behind the HSEG transaction address is not remapped and is not accessible. All cacheline writes with WB attribute or Implicit write backs to the HSEG range are completed to DRAM like an SMM cycle.

3.3.3 FSB Interrupt Memory Space (FEE0_0000 – FEEF_FFFF)

The FSB Interrupt space is the address used to deliver interrupts to the FSB. Any device on PCI Express or DMI may issue a Memory Write to 0FEEx_xxxxh. The MCH will forward this Memory Write along with the data to the FSB as an Interrupt Message Transaction. The MCH terminates the FSB transaction by providing the response and asserting HTRDYB. This Memory Write cycle does not go to DRAM.

3.3.4 High BIOS Area

The top 2 MB (FFE0_0000h – FFFF_FFFFh) of the PCI Memory Address Range is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The processor begins execution from the High BIOS after reset. This region is mapped to DMI Interface so that the upper subset of this region aliases to 16 MB-256 KB range. The actual address space required for the BIOS is less than 2 MB but the minimum processor MTRR range for this region is 2 MB so that full 2 MB must be considered.

3.4 Main Memory Address Space (4 GB to TOUUD)

The MCH supports 36 bit addressing. The maximum main memory size supported is 8 GB total DRAM memory. A hole between TOLUD and 4 G occurs when main memory size approaches 4 GB or larger. As a result, TOM, and TOUUD registers and RECLAIMBASE/RECLAIMLIMIT registers become relevant.

The new reclaim configuration registers exist to reclaim lost main memory space. The greater than 32 bit reclaim handling will be handled similar to other MCHs.

Upstream read and write accesses above 36-bit addressing will be treated as invalid cycles by PCI Express and DMI.

Top of Memory

The “Top of Memory” (TOM) register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped I/O above TOM). TOM is used to allocate the Intel Management Engine's stolen memory. The Intel ME stolen size register reflects the total amount of physical memory stolen by the Intel ME. The ME stolen memory is located at the top of physical memory. The ME stolen memory base is calculated by subtracting the amount of memory stolen by the Intel ME from TOM.

The Top of Upper Usable Dram (TOUUD) register reflects the total amount of addressable DRAM. If reclaim is disabled, TOUUD will reflect TOM minus Intel ME stolen size. If reclaim is enabled, then it will reflect the reclaim limit. Also, the reclaim base will be the same as TOM minus ME stolen memory size to the nearest 64 MB alignment.

TOLUD register is restricted to 4 GB memory (A[31:20]), but the MCH can support up to 16 GB, limited by DRAM pins. For physical memory greater than 4 GB, the TOUUD register helps identify the address range in between the 4 GB boundary and the top of physical memory. This identifies memory that can be directly accessed (including reclaim address calculation) which is useful for memory access indication, early path indication, and trusted read indication. When reclaim is enabled, TOLUD must be 64 MB aligned, but when reclaim is disabled, TOLUD can be 1 MB aligned.

C1DRB3 cannot be used directly to determine the effective size of memory as the values programmed in the DRBs depend on the memory mode (stacked, interleaved). The Reclaim Base/Limit registers also can not be used because reclaim can be disabled. The C0DRB3 register is used for memory channel identification (channel 0 vs. channel 1) in the case of stacked memory.

3.4.1 Memory Re-claim Background

The following are examples of Memory Mapped I/O devices are typically located below 4 GB:

- High BIOS
- HSEG
- TSEG
- XAPIC
- Local APIC
- FSB Interrupts
- Mbase/Mlimit
- Memory Mapped IO space that supports only 32 B addressing

The MCH provides the capability to re-claim the physical memory overlapped by the Memory Mapped I/O logical address space. The MCH re-maps physical memory from the Top of Low Memory (TOLUD) boundary up to the 4 GB boundary to an equivalent sized logical address range located just below the Intel ME's stolen memory.

3.4.2 Memory Reclaiming

An incoming address (referred to as a logical address) is checked to see if it falls in the memory re-map window. The bottom of the re-map window is defined by the value in the RECLAIMBASE register. The top of the re-map window is defined by the value in the RECLAIMLIMIT register. An address that falls within this window is reclaimed to the physical memory starting at the address defined by the TOLUD register. The TOLUD register must be 64 MB aligned when RECLAIM is enabled, but can be 1 MB aligned when reclaim is disabled.

3.5 PCI Express* Configuration Address Space

There is a device 0 register, PCIEXBAR, which defines the base address for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. The size of this range will be programmable for the MCH. BIOS must assign this address range such that it will not conflict with any other address ranges.

See the configuration portion of this document for more details.

3.6 PCI Express* Address Space

The MCH can be programmed to direct memory accesses to the PCI Express interface when addresses are within either of two ranges specified via registers in MCH's Device 1 configuration space.

- The first range is controlled via the Memory Base Register (MBASE) and Memory Limit Register (MLIMIT) registers.
- The second range is controlled via the Pre-fetchable Memory Base (PMBASE) and Pre-fetchable Memory Limit (PMLIMIT) registers.

Conceptually, address decoding for each range follows the same basic concept. The top 12 bits of the respective Memory Base and Memory Limit registers correspond to address bits A[31:20] of a memory address. For the purpose of address decoding, the MCH assumes that address bits A[19:0] of the memory base are zero and that address bits A[19:0] of the memory limit address are FFFFFh. This forces each memory address range to be aligned to 1 MB boundary and to have a size granularity of 1 MB.

The MCH positively decodes memory accesses to PCI Express memory address space as defined by the following equations:

Memory_Base_Address ≤ Address ≤ Memory_Limit_Address

Prefetchable_Memory_Base_Address ≤ Address ≤ Prefetchable_Memory_Limit_Address

The window size is programmed by the plug-and-play configuration software. The window size depends on the size of memory claimed by the PCI Express device. Normally these ranges will reside above the Top-of-Low Usable-DRAM and below High BIOS and APIC address ranges. They MUST reside above the top of low memory (TOLUD) if they reside below 4 GB and MUST reside above top of upper memory (TOUUD) if they reside above 4 GB or they will steal physical DRAM memory space.

It is essential to support a separate Pre-fetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note that the MCH Device 1 memory range registers described above are used to allocate memory address space for any PCI Express devices sitting on PCI Express that require such a window.

The PCICMD1 register can override the routing of memory accesses to PCI Express. In other words, the memory access enable bit must be set in the device 1 PCICMD1 register to enable the memory base/limit and pre-fetchable base/limit windows.

For the MCH, the upper PMUBASE1/PMULIMIT1 registers have been implemented for PCI Express Spec compliance. The MCH locates MMIO space above 4 GB using these registers.

3.7 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SMM RAM). The MCH supports: Compatible SMRAM (C_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. MCH provides three SMRAM options:

- Below 1 MB option that supports compatible SMI handlers.
- Above 1 MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional TSEG area of 1 MB, 2 MB, or 8 MB in size. The TSEG area lies below stolen memory.

The above 1 MB solutions require changes to compatible SMRAM handlers code to properly execute above 1 MB.

Note: DMI Interface and PCI Express masters are not allowed to access the SMM space.

3.7.1 SMM Space Definition

SMM space is defined by its **addressed** SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the processor to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High and TSEG. The Compatible and TSEG SMM space is not remapped and therefore the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DRAM SMM space is a different address range. Note that the High DRAM space is the same as the Compatible Transaction Address space. Table 6 describes three unique address ranges:

- Compatible Transaction Address
- High Transaction Address
- TSEG Transaction Address

Table 6. Transaction Address Ranges – Compatible, High, and TSEG

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
Compatible	000A_0000h to 000B_FFFFh	000A_0000h to 000B_FFFFh
High	FEDA_0000h to FEDB_FFFFh	000A_0000h to 000B_FFFFh
TSEG	(TOLUD–STOLEN–TSEG) to TOLUD–STOLEN	(TOLUD–STOLEN–TSEG) to TOLUD–STOLEN

3.7.2 SMM Space Restrictions

If any of the following conditions are violated the results of SMM accesses are unpredictable and may cause the system to hang:

1. The Compatible SMM space **must not** be set-up as cacheable.
2. High or TSEG SMM transaction address space **must not** overlap address space assigned to system DRAM, or to any "PCI" devices (including DMI Interface, PCI-Express). This is a BIOS responsibility.
3. Both D_OPEN and D_CLOSE **must not** be set to 1 at the same time.
4. When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available DRAM. This is a BIOS responsibility.
5. Any address translated through the GMADR TLB must not target DRAM from A_0000h–F_FFFFh.

3.7.3 SMM Space Combinations

When High SMM is enabled (G_SMRAME=1 and H_SMRAM_EN=1), the Compatible SMM space is effectively disabled. processor originated accesses to the Compatible SMM space are forwarded to PCI Express; otherwise, they are forwarded to the DMI Interface. PCI Express and DMI Interface originated accesses are **never** allowed to access SMM space.

Table 7. SMM Space

Global Enable G_SMRAME	High Enable H_SMRAM_EN	TSEG Enable TSEG_EN	Compatible (C) Range	High (H) Range	TSEG (T) Range
0	X	X	Disable	Disable	Disable
1	0	0	Enable	Disable	Disable
1	0	1	Enable	Disable	Enable
1	1	0	Disabled	Enable	Disable
1	1	1	Disabled	Enable	Enable

3.7.4 SMM Control Combinations

The G_SMRAME bit provides a global enable for all SMM memory. The D_OPEN bit allows software to write to the SMM ranges without being in SMM mode. BIOS software can use this bit to initialize SMM code at powerup. The D_LCK bit limits the SMM range access to only SMM mode accesses. The D_CLS bit causes SMM (both CSEG and TSEG) data accesses to be forwarded to the DMI Interface or PCI Express. The SMM software can use this bit to write to video memory while running SMM code out of DRAM.

Table 8. SMM Control Table

G_SMRAME	D_LCK	D_CLS	D_OPEN	Processor in SMM Mode	SMM Code Access	SMM Data Access
0	x	X	x	x	Disable	Disable
1	0	X	0	0	Disable	Disable
1	0	0	0	1	Enable	Enable
1	0	0	1	x	Enable	Enable
1	0	1	0	1	Enable	Disable
1	0	1	1	x	Invalid	Invalid
1	1	X	x	0	Disable	Disable
1	1	0	x	1	Enable	Enable
1	1	1	x	1	Enable	Disable

3.7.5 SMM Space Decode and Transaction Handling

Only the processor is allowed to access SMM space. PCI Express and DMI Interface originated transactions are not allowed to SMM space.

3.7.6 Processor WB Transaction to an Enabled SMM Address Space

Processor Writeback transactions (REQa[1]# = 0) to enabled SMM Address Space must be written to the associated SMM DRAM even though D_OPEN=0 and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.

3.7.7 SMM Access Through TLB

Accesses through TLB address translation to enabled SMM DRAM space are not allowed. Writes will be routed to Memory address 000C_0000h with byte enables de-asserted and reads will be routed to Memory address 000C_0000h. If a TLB translated address hits enabled SMM DRAM space, an error is recorded.

PCI Express and DMI Interface originated accesses are **never** allowed to access SMM space directly or through the TLB address translation. If a TLB translated address hits enabled SMM DRAM space, an error is recorded.

PCI Express and DMI Interface write accesses through GMADR range will be snooped. Assesses to GMADR linear range (defined via fence registers) are supported. PCI Express and DMI Interface writes to GMADR are not supported. If, when translated, the resulting physical address is to enabled SMM DRAM space, the request will be remapped to address 000C_0000h with de-asserted byte enables.

PCI Express and DMI Interface read accesses to the GMADR range are not supported therefore will have no address translation concerns. PCI Express and DMI Interface reads to GMADR will be remapped to address 000C_0000h. The read will complete with UR (unsupported request) completion status.

Fetches are always decoded (at fetch time) to ensure not in SMM (actually, anything above base of TSEG or 640 KB – 1 MB). Thus, they will be invalid and go to address 000C_0000h, but that isn't specific to PCI Express or DMI; it applies to the processor. Also, since the GMADR snoop would not be directly to the SMM space, there wouldn't be a writeback to SMM. In fact, the writeback would also be invalid (because it uses the same translation) and go to address 000C_0000h.

3.8 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be "shadowed" into MCH DRAM memory. Typically this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as a read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. Processor bus transactions are routed accordingly.

3.9 I/O Address Space

The MCH does not support the existence of any other I/O devices beside itself on the processor bus. The MCH generates either DMI Interface or PCI Express bus cycles for all processor I/O accesses that it does not claim. Within the host bridge, the MCH contains two internal registers in the processor I/O space, Configuration Address Register (CONFIG_ADDRESS) and the Configuration Data Register (CONFIG_DATA). These locations are used to implement configuration space access mechanism.

The processor allows 64 K+3 bytes to be addressed within the I/O space. The MCH propagates the processor I/O address without any translation on to the destination bus and therefore provides addressability for 64K+3 byte locations. Note that the upper 3 locations can be accessed only during I/O address wrap-around when processor bus HAB_16 address signal is asserted. HAB_16 is asserted on the processor bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. HAB_16 is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI Interface bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are NOT posted. Memory writes to ICH or PCI Express are posted. The PCICMD1 register can disable the routing of I/O cycles to the PCI Express.

The MCH responds to I/O cycles initiated on PCI Express or DMI with an UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the request will route as a read to Memory address 000C_0000h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with an UR completion status.

I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the processor as 1 transaction. The MCH will break this into 2 separate transactions. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries are assumed to be split into 2 transactions by the processor.

3.9.1 PCI Express* I/O Address Mapping

The MCH can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when processor initiated I/O cycle addresses are within the PCI Express I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in MCH Device 1 configuration space.

Address decoding for this range is based on the following concept. The top 4 bits of the respective I/O Base and I/O Limit registers correspond to address bits A[15:12] of an I/O address. For the purpose of address decoding, the MCH assumes that lower 12 address bits A[11:0] of the I/O base are zero and that address bits A[11:0] of the I/O limit address are FFFh. This forces the I/O address range alignment to 4 KB boundary and produces a size granularity of 4 KB.

The MCH positively decodes I/O accesses to PCI Express I/O address space as defined by the following equation:

I/O_Base_Address ≤ Processor I/O Cycle Address ≤ I/O_Limit_Address

The effective size of the range is programmed by the plug-and-play configuration software and it depends on the size of I/O space claimed by the PCI Express device.

Note that the MCH Device 1 and/or Device 6 I/O address range registers defined above are used for all I/O space allocation for any devices requiring such a window on PCI Express.

The PCICMD1 register can disable the routing of I/O cycles to PCI Express.

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4 MCH Register Description

The MCH contains two sets of software accessible registers, accessed via the Host processor I/O address space: Control registers and internal configuration registers.

- Control registers are I/O mapped into the processor I/O space, which control access to PCI and PCI Express configuration space (see Section 6).
- Internal configuration registers residing within the MCH are partitioned into two logical device register sets ("logical" since they reside within a single physical device). The first register set is dedicated to Host Bridge functionality (i.e., DRAM configuration, other chipset operating parameters, and optional features). The second register block is dedicated to Host-to-PCI Express Bridge functions (controls PCI Express interface configurations and operating parameters).

The MCH internal registers (I/O Mapped, Configuration, and PCI Express Extended Configuration registers) are accessible by the processor. The registers that reside within the lower 256 bytes of each device can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFIG_ADDRESS, which can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). Registers which reside in bytes 256 through 4095 of each device may only be accessed using memory-mapped transactions in DWord (32-bit) quantities.

Some of the MCH registers described in this section contain reserved bits. These bits are labeled "Reserved". Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, and write operation for the Configuration Address Register.

In addition to reserved bits within a register, the MCH contains address locations in the configuration space of the Host Bridge entity that are marked either "Reserved" or "Intel Reserved". The MCH responds to accesses to "Reserved" address locations by completing the host cycle. When a "Reserved" register location is read, a zero value is returned. ("Reserved" registers can be 8-, 16-, or 32-bits in size). Writes to "Reserved" registers have no effect on the MCH. Registers that are marked as "Intel Reserved" must not be modified by system software. Writes to "Intel Reserved" registers may cause system failure. Reads from "Intel Reserved" registers may return a non-zero value.

Upon a Full Reset, the MCH sets its entire set of internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bringing up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the MCH registers accordingly.

4.1 Register Terminology

The following table shows the register-related terminology that is used.

Item	Description
RO	Read Only bit(s). Writes to these bits have no effect.
RO/S	Read Only / Sticky. Writes to these bits have no effect. These are status bits only. Bits are not returned to their default values by “warm” reset, but will be reset with a cold/complete reset (for PCI Express related bits, a cold reset is “Power Good Reset” as defined in the PCI Express specification).
RS/WC	Read Set / Write Clear bit(s). These bits are set to ‘1’ when read and then will continue to remain set until written. A write of ‘1’ clears (sets to ‘0’) the corresponding bit(s) and a write of ‘0’ has no effect.
R/W	Read / Write bit(s). These bits can be read and written.
R/WC	Read / Write Clear bit(s). These bits can be read. Internal events may set this bit. A write of ‘1’ clears (sets to ‘0’) the corresponding bit(s) and a write of ‘0’ has no effect.
R/WC/S	Read / Write Clear / Sticky bit(s). These bits can be read. Internal events may set this bit. A write of ‘1’ clears (sets to ‘0’) the corresponding bit(s) and a write of ‘0’ has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the *PCI Express Specification*).
R/W/L	Read / Write / Lockable bit(s). These bits can be read and written. Additionally, there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/W/K	Read / Write / Key bit(s). These bits can be read and written by software. Additionally this bit when set, prohibits some other bit field(s) from being writeable (bit fields become Read Only).
R/W/L	Read / Write / Lockable bit(s). These bits can be read and written. Additionally there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/W/S	Read / Write / Sticky bit(s). These bits can be read and written. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the *PCI Express Specification*).
R/WSC	Read / Write Self Clear bit(s). These bits can be read and written. When the bit is ‘1’, hardware may clear the bit to ‘0’ based upon internal events, possibly sooner than any subsequent read could retrieve a ‘1’.
R/WSC/L	Read / Write Self Clear / Lockable bit(s). These bits can be read and written. When the bit is ‘1’, hardware may clear the bit to ‘0’ based upon internal events, possibly sooner than any subsequent read could retrieve a ‘1’. Additionally there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/WO	Write Once bit(s). Once written, bits with this attribute become Read Only. These bits can only be cleared by a Reset.
W	Write Only. Whose bits may be written, but will always-return zeros when read. They are used for write side effects. Any data written to these registers cannot be retrieved.

4.2 Configuration Process and Registers

4.2.1 Platform Configuration Structure

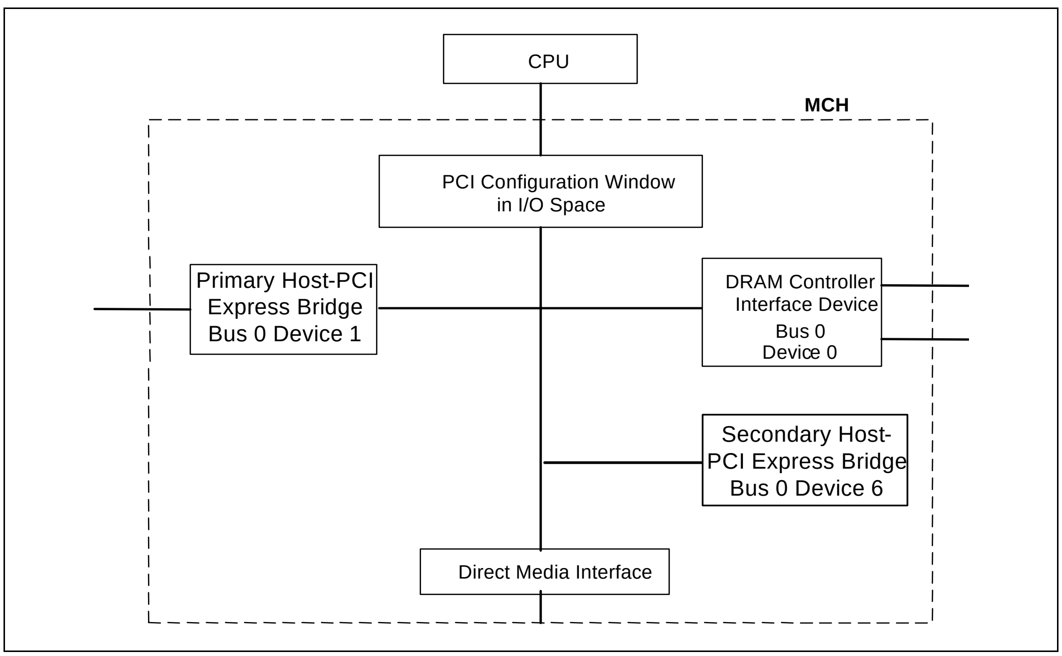
The DMI physically connects the MCH and the Intel ICH9; thus, from a configuration standpoint, the DMI is logically PCI bus 0. As a result, all devices internal to the MCH and the ICH appear to be on PCI bus 0.

Note: The ICH9 internal LAN controller does not appear on bus 0 – it appears on the external PCI bus and this number is configurable.

The system's primary PCI expansion bus is physically attached to the ICH and from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge; therefore, it has a programmable PCI Bus number. The PCI Express Interface appears to system software to be a real PCI bus behind a PCI-to-PCI bridge that is a device resident on PCI bus 0.

Note: A physical PCI bus 0 does not exist; DMI and the internal devices in the MCH and ICH logically constitute PCI Bus 0 to configuration software. This is shown in Figure 6.

Figure 6. Conceptual Intel® X48 Platform PCI Configuration Diagram



The MCH contains four PCI devices within a single physical component. The configuration registers for the four devices are mapped as devices residing on PCI bus 0.

- **Device 0: Host Bridge / DRAM Controller.** Logically this appears as a PCI device residing on PCI bus 0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), and configuration for the DMI and other MCH specific registers.
- **Device 1: Primary Host-PCI Express Bridge**. Logically this appears as a “virtual” PCI-to-PCI bridge residing on PCI bus 0 and is compliant with *PCI Express Specification* Revision 2.0. Device 1 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers (including the PCI Express memory address mapping). It also contains Isochronous and Virtual Channel controls in the PCI Express extended configuration space.
- **Device 6: Secondary Host-PCI Express Bridge**. Logically this appears as a “virtual” PCI-to-PCI bridge residing on PCI bus 0 and is compliant with *PCI Express Specification* Revision 2.0. Device 6 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers (including the PCI Express memory address mapping). It also contains Isochronous and Virtual Channel controls in the PCI Express extended configuration space.

4.3 Configuration Mechanisms

The processor is the originator of configuration cycles so the FSB is the only interface in the platform where these mechanisms are used. The MCH translates transactions received through both configuration mechanisms to the same format.

4.3.1 Standard PCI Configuration Mechanism

The following is the mechanism for translating processor I/O bus cycles to configuration cycles.

The PCI specification defines a slot based "configuration space" that allows each device to contain up to 8 functions with each function containing up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the MCH.

The configuration access mechanism makes use of the CONFIG_ADDRESS Register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA Register (at I/O address 0CFCh though 0CFFh). To reference a configuration register a DWord I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device and a specific configuration register of the device function being accessed. CONFIG_ADDRESS[31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the MCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The MCH is responsible for translating and routing the processor’s I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal MCH configuration registers, DMI or PCI Express.

4.3.2 PCI Express Enhanced Configuration Mechanism

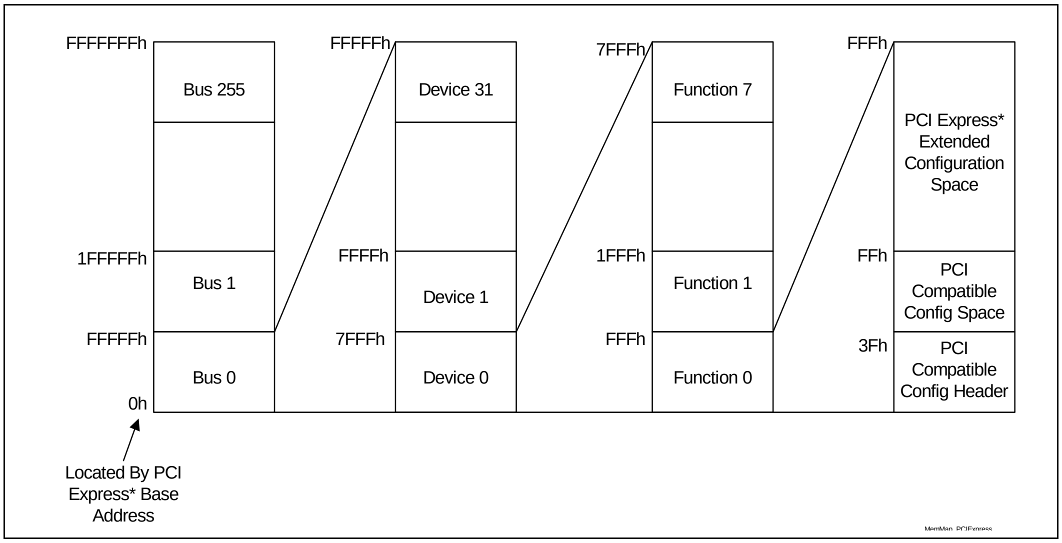
PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by PCI Specification Revision 2.3. PCI Express configuration space is divided into a PCI 2.3 compatible region, which consists of the first 256B of a logical device's configuration space and a PCI Express extended region, which consists of the remaining configuration space.

The PCI compatible region can be accessed using either the Standard PCI Configuration Mechanism or using the PCI Express Enhanced Configuration Mechanism described in this section. The extended configuration registers may only be accessed using the PCI Express Enhanced Configuration Mechanism. To maintain compatibility with PCI configuration addressing mechanisms, system software must access the extended configuration space using 32-bit operations (32-bit aligned) only. These 32-bit operations include byte enables allowing only appropriate bytes within the DWord to be accessed. Locked transactions to the PCI Express memory mapped configuration address space are not supported. All changes made using either access mechanism are equivalent.

The PCI Express Enhanced Configuration Mechanism utilizes a flat memory-mapped address space to access device configuration registers. This address space is reported by the system firmware to the operating system. There is a register, PCIEXBAR, that defines the base address for the block of addresses below 4 GB for the configuration space associated with busses, devices and functions that are potentially a part of the PCI Express root complex hierarchy. In the PCIEXBAR register there exists controls to limit the size of this reserved memory mapped space. 256 MB is the amount of address space required to reserve space for every bus, device, and function that could possibly exist. Options for 128 MB and 64 MB exist in order to free up those addresses for other uses. In these cases the number of busses and all of their associated devices and functions are limited to 128 or 64 busses respectively.

The PCI Express Configuration Transaction Header includes an additional 4 bits (ExtendedRegisterAddress[3:0]) between the Function Number and Register Address fields to provide indexing into the 4 KB of configuration space allocated to each potential device. For PCI Compatible Configuration Requests, the Extended Register Address field must be all zeros.

Figure 7. Memory Map to PCI Express Device Configuration Space



As with PCI devices, each device is selected based on decoded address information that is provided as a part of the address portion of Configuration Request packets. A PCI Express device will decode all address information fields (bus, device, function and extended address numbers) to provide access to the correct register.

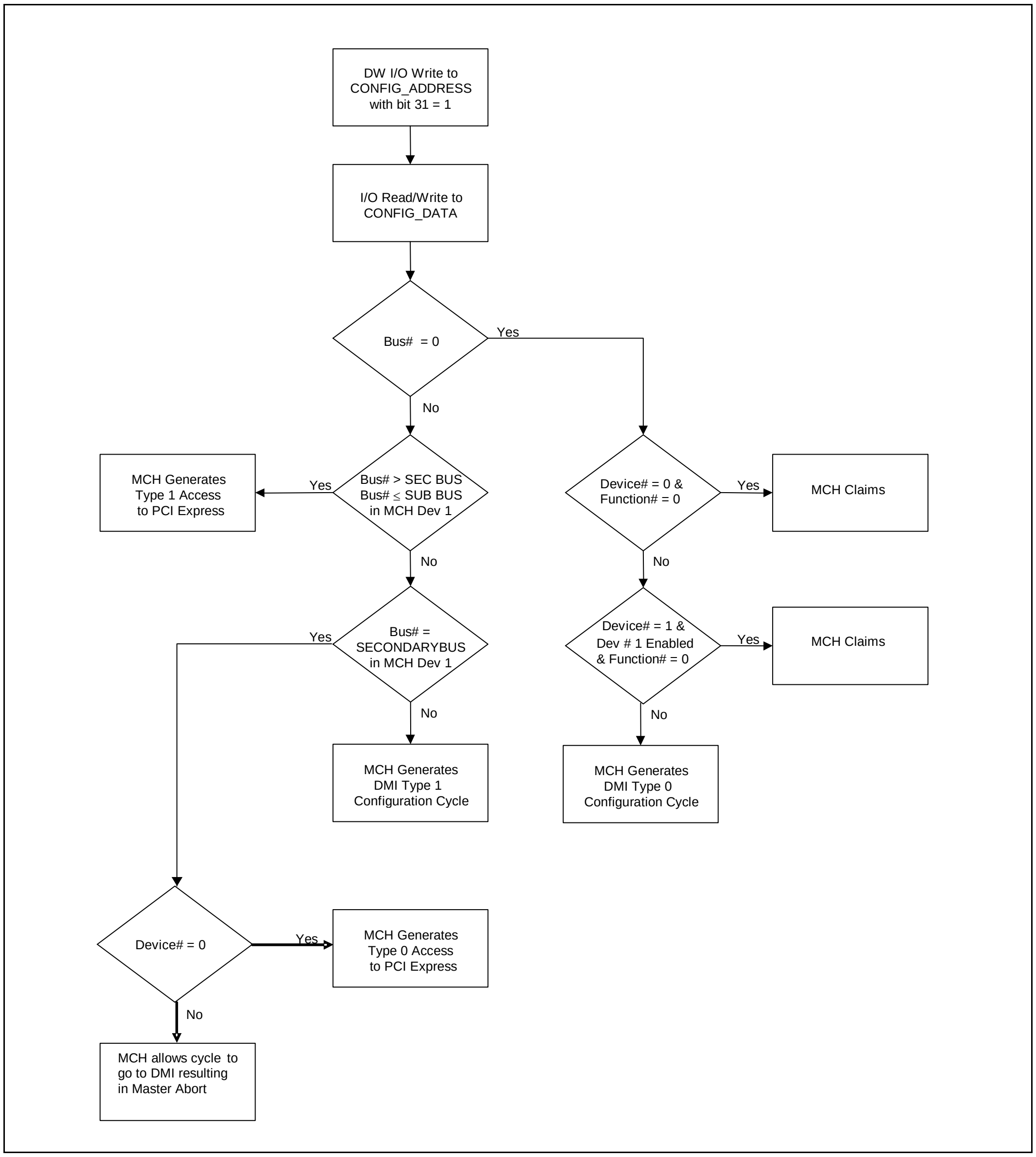
To access this space (steps 1, 2, 3 are done only once by BIOS):

1. Use the PCI compatible configuration mechanism to enable the PCI Express enhanced configuration mechanism by writing 1 to bit 0 of the PCIEXBAR register.
2. Use the PCI compatible configuration mechanism to write an appropriate PCI Express base address into the PCIEXBAR register.
3. Calculate the host address of the register you wish to set using (PCI Express base + (bus number * 1 MB) + (device number * 32KB) + (function number * 4 KB) + (1 B * offset within the function) = host address).
4. Use a memory write or memory read cycle to the calculated host address to write or read that register.

4.4 Routing Configuration Accesses

The MCH supports two PCI related interfaces: DMI and PCI Express. The MCH is responsible for routing PCI and PCI Express configuration cycles to the appropriate device that is an integrated part of the MCH or to one of these two interfaces. Configuration cycles to the ICH internal devices and Primary PCI (including downstream devices) are routed to the ICH via DMI. Configuration cycles to the PCI Express PCI compatibility configuration space are routed to the PCI Express port device or associated link.

Figure 8. MCH Configuration Cycle Flow Chart



4.4.1 Internal Device Configuration Accesses

The MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0 the configuration cycle is targeting a PCI Bus #0 device.

If the targeted PCI Bus #0 device exists in the MCH and is not disabled, the configuration cycle is claimed by the appropriate device.

4.4.2 Bridge Related Configuration Accesses

Configuration accesses on PCI Express or DMI are PCI Express Configuration TLPs (Transaction Layer Packets):

- Bus Number [7:0] is Header Byte 8 [7:0]
- Device Number [4:0] is Header Byte 9 [7:3]
- Function Number [2:0] is Header Byte 9 [2:0]

And special fields for this type of TLP:

- Extended Register Number [3:0] is Header Byte 10 [3:0]
- Register Number [5:0] is Header Byte 11 [7:2]

See the PCI Express specification for more information on both the PCI 2.3 compatible and PCI Express Enhanced Configuration Mechanism and transaction rules.

4.4.2.1 PCI Express Configuration Accesses

When the Bus Number of a type 1 Standard PCI Configuration cycle or PCI Express Enhanced Configuration access matches the Device 1 Secondary Bus Number a PCI Express Type 0 Configuration TLP is generated on the PCI Express link targeting the device directly on the opposite side of the link. This should be Device 0 on the bus number assigned to the PCI Express link (likely Bus #1).

The device on other side of link must be Device 0. The MCH will Master Abort any Type 0 Configuration access to a non-zero Device number. If there is to be more than one device on that side of the link there must be a bridge implemented in the downstream device.

When the Bus Number of a type 1 Standard PCI Configuration cycle or PCI Express Enhanced Configuration access is within the claimed range (between the upper bound of the bridge device's Subordinate Bus Number register and the lower bound of the bridge device's Secondary Bus Number register) but doesn't match the Device 1 Secondary Bus Number, a PCI Express Type 1 Configuration TLP is generated on the secondary side of the PCI Express link.

PCI Express Configuration Writes:

- Internally the host interface unit will translate writes to PCI Express extended configuration space to configuration writes on the backbone.
- Writes to extended space are posted on the FSB, but non-posted on the PCI Express or DMI (i.e., translated to config writes)

4.4.2.2 DMI Configuration Accesses

Accesses to disabled MCH internal devices, bus numbers not claimed by the Host-PCI Express bridge, or PCI Bus #0 devices not part of the MCH will subtractively decode to the ICH and consequently be forwarded over the DMI via a PCI Express configuration TLP.

If the Bus Number is zero, the MCH will generate a Type 0 Configuration Cycle TLP on DMI. If the Bus Number is non-zero, and falls outside the range claimed by the Host-PCI Express bridge, the MCH will generate a Type 1 Configuration Cycle TLP on DMI.

The ICH routes configurations accesses in a manner similar to the MCH. The ICH decodes the configuration TLP and generates a corresponding configuration access. Accesses targeting a device on PCI Bus #0 may be claimed by an internal device. The ICH compares the non-zero Bus Number with the Secondary Bus Number and

Subordinate Bus Number registers of its PCI-to-PCI bridges to determine if the configuration access is meant for Primary PCI, or some other downstream PCI bus or PCI Express link.

Configuration accesses that are forwarded to the ICH9, but remain unclaimed by any device or bridge will result in a master abort.

4.5 MCH Register Introduction

4.6 I/O Mapped Registers

The MCH contains two registers that reside in the processor I/O address space – the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

4.6.1 CONFIG_ADDRESS—Configuration Address Register

I/O Address: 0CF8h Accessed as a DW
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a DW. A Byte or Word reference will "pass through" the Configuration Address Register and DMI onto the Primary PCI bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Access & Default	Description
31	R/W 0b	**Configuration Enable (CFGE)** 0 = Disable 1 = Enable
30:24		Reserved
23:16	R/W 00h	**Bus Number:** If the Bus Number is programmed to 00h the target of the Configuration Cycle is a PCI Bus 0 agent. If this is the case and the MCH is not the target (i.e., the device number is ≥ 2), then a DMI Type 0 Configuration Cycle is generated. If the Bus Number is non-zero and does not fall within the ranges enumerated by device 1's Secondary Bus Number or Subordinate Bus Number Register, then a DMI Type 1 Configuration Cycle is generated. If the Bus Number is non-zero and matches the value programmed into the Secondary Bus Number Register of device 1, a Type 0 PCI configuration cycle will be generated on PCI Express. If the Bus Number is non-zero, greater than the value in the Secondary Bus Number register of device 1 and less than or equal to the value programmed into the Subordinate Bus Number Register of device 1 a Type 1 PCI configuration cycle will be generated on PCI Express. This field is mapped to byte 8 [7:0] of the request header format during PCI Express Configuration cycles and A[23:16] during the DMI Type 1 configuration cycles.

Bit	Access & Default	Description
15:11	R/W 00h	**Device Number:** This field allows the configuration registers of a particular function in a multi-function device to be accessed. The MCH ignores configuration cycles to its internal devices if the function number is not equal to 0 or 1. This field is mapped to byte 6 [2:0] of the request header format during PCI Express Configuration cycles and A[10:8] during the DMI configuration cycles.
10:8	R/W 000b	**Function Number:** This field allows the configuration registers of a particular function in a multi-function device to be accessed. The MCH ignores configuration cycles to its internal devices if the function number is not equal to 0 or 1. This field is mapped to byte 6 [2:0] of the request header format during PCI Express Configuration cycles and A[10:8] during the DMI configuration cycles.
7:2	R/W 00h	**Register Number:** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to byte 7 [7:2] of the request header format during PCI Express Configuration cycles and A[7:2] during the DMI Configuration cycles.
1:0		Reserved

4.6.2 CONFIG_DATA—Configuration Data Register

I/O Address: 0CFCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Access & Default	Description
31:0	R/W 0000 0000h	**Configuration Data Window (CDW):** If bit 31 of CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register will produce a configuration transaction using the contents of CONFIG_ADDRESS to determine the bus, device, function, and offset of the register to be accessed.

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5 DRAM Controller Registers (D0:F0)

The DRAM Controller registers are in Device 0 (D0), Function 0 (F0).

Warning: Address locations that are not listed are considered Intel Reserved registers locations. Reads to Reserved registers may return non-zero values. Writes to reserved locations may cause system failures.

All registers that are defined in the PCI 2.3 specification, but are not necessary or implemented in this component are simply not included in this document. The reserved/unimplemented space in the PCI configuration header space is not documented as such in this summary.

Table 9. DRAM Controller Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
0–1h	VID	Vendor Identification	8086h	RO
2–3h	DID	Device Identification	29E0h	RO
4–5h	PCICMD	PCI Command	0006h	RO, RW
6–7h	PCISTS	PCI Status	0090h	RO, RWC
8h	RID	Revision Identification	see register description	RO
9–Bh	CC	Class Code	060000h	RO
Dh	MLT	Master Latency Timer	00h	RO
Eh	HDR	Header Type	00h	RO
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	RWO
2E–2Fh	SID	Subsystem Identification	0000h	RWO
34h	CAPPTR	Capabilities Pointer	E0h	RO
40–47h	PXPEPBAR	PCI Express Egress Port Base Address	0000000000 000000h	RO, RW/L
48–4Fh	MCHBAR	MCH Memory Mapped Register Range Base	0000000000 000000h	RO, RW/L
54–57h	DEVEN	Device Enable	000023DBh	RO, RW/L
60–67h	PCIEXBAR	PCI Express Register Range Base Address	00000000E0 000000h	RO, RW/L, RW/L/K
68–6Fh	DMIBAR	Root Complex Register Range Base Address	0000000000 000000h	RO, RW/L
90h	PAM0	Programmable Attribute Map 0	00h	RO, RW/L
91h	PAM1	Programmable Attribute Map 1	00h	RO, RW/L
92h	PAM2	Programmable Attribute Map 2	00h	RO, RW/L
93h	PAM3	Programmable Attribute Map 3	00h	RO, RW/L
94h	PAM4	Programmable Attribute Map 4	00h	RO, RW/L

Table 9. DRAM Controller Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
95h	PAM5	Programmable Attribute Map 5	00h	RO, RW/L
96h	PAM6	Programmable Attribute Map 6	00h	RO, RW/L
97h	LAC	Legacy Access Control	00h	RW, RW/L, RO
98–99h	REMAPBASE	Remap Base Address Register	03FFh	RO, RW/L
9A–9Bh	REMAPLIMIT	Remap Limit Address Register	0000h	RO, RW/L
9Dh	SMRAM	System Management RAM Control	02h	RO, RW/L, RW, RW/L/K
9Eh	ESMRAMC	Extended System Management RAM Control	38h	RW/L, RWC, RO
A0–A1h	TOM	Top of Memory	0001h	RO, RW/L
A2–A3h	TOUUD	Top of Upper Usable Dram	0000h	RW/L
A4–A7h	BSM	Base of Stolen Memory	00000000h	RW/L, RO
AC–AFh	TSEGMB	TSEG Memory Base	00000000h	RO, RW/L
B0–B1h	TOLUD	Top of Low Usable DRAM	0010h	RW/L, RO
C8–C9h	ERRSTS	Error Status	0000h	RWC/S, RO
CA–CBh	ERRCMD	Error Command	0000h	RW, RO
CC–CDh	SMICMD	SMI Command	0000h	RO, RW
DC–DFh	SKPD	Scratchpad Data	00000000h	RW
E0–EBh	CAPID0	Capability Identifier	0000000181 064000010C 0009h	RO

5.1 Configuration Register Details

5.1.1 VID—Vendor Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 0–1h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

5.1.2 DID—Device Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 2–3h
Default Value: 29E0h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:0	RO	29E0h	**Device Identification Number (DID):** This field identifier assigned to the MCH core/primary PCI device.

5.1.3 PCICMD—PCI Command

B/D/F/Type: 0/0/0/PCI
Address Offset: 4–5h
Default Value: 0006h
Access: RO, RW
Size: 16 bits

Since MCH Device 0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Access	Default Value	Description
15:9	RO	00h	Reserved
8	RW	0b	**SERR Enable (SERRE):** This bit is a global enable bit for Device 0 SERR messaging. The MCH does not have an SERR signal. The MCH communicates the SERR condition by sending an SERR message over DMI to the ICH. 1 = The MCH is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD and DMIUEMSK registers. The error status is reported in the ERRSTS, PCISTS, and DMIUEST registers. 0 = The SERR message is not generated by the MCH for Device 0. Note that this bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring in that device. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism.
7	RO	0b	**Address/Data Stepping Enable (ADSTEP):** Address/data stepping is not implemented in the MCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	RW	0b	**Parity Error Enable (PERRE):** Controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0 = Master Data Parity Error bit in PCI Status register can NOT be set. 1 = Master Data Parity Error bit in PCI Status register CAN be set.
5	RO	0b	Reserved
4	RO	0b	**Memory Write and Invalidate Enable (MWIE):** The MCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	RO	0b	Reserved
2	RO	1b	**Bus Master Enable (BME):** The MCH is always enabled as a master on the backbone. This bit is hardwired to a "1". Writes to this bit position have no effect.
1	RO	1b	**Memory Access Enable (MAE):** The MCH always allows access to main memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	RO	0b	**I/O Access Enable (IOAE):** This bit is not implemented in the MCH and is hardwired to a 0. Writes to this bit position have no effect.

5.1.4 PCISTS—PCI Status

B/D/F/Type: 0/0/0/PCI
Address Offset: 6–7h
Default Value: 0090h
Access: RO, RWC
Size: 16 bits

This status register reports the occurrence of error events on Device 0's PCI interface. Since the MCH Device 0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Access	Default Value	Description
15	RWC	0b	**Detected Parity Error (DPE):** This bit is set when this Device receives a Poisoned TLP.
14	RWC	0b	**Signaled System Error (SSE):** This bit is set to 1 when the MCH Device 0 generates an SERR message over DMI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD, ERRCMD, and DMIUEMSK registers. Device 0 error flags are read/reset from the PCISTS, ERRSTS, or DMIUEST registers. Software clears this bit by writing a 1 to it.
13	RWC	0b	**Received Master Abort Status (RMAS):** This bit is set when the MCH generates a DMI request that receives an Unsupported Request completion packet. Software clears this bit by writing a 1 to it.
12	RWC	0b	**Received Target Abort Status (RTAS):** This bit is set when the MCH generates a DMI request that receives a Completer Abort completion packet. Software clears this bit by writing a 1 to it.
11	RO	0b	**Signaled Target Abort Status (STAS):** The MCH will not generate a Target Abort DMI completion packet or Special Cycle. This bit is not implemented in the MCH and is hardwired to a 0. Writes to this bit position have no effect.
10:9	RO	00b	**DEVSEL Timing (DEVT):** These bits are hardwired to "00". Writes to these bit positions have no affect. Device 0 does not physically connect to PCI_A. These bits are set to "00" (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the MCH.
8	RWC	0b	**Master Data Parity Error Detected (DPD):** This bit is set when DMI received a Poisoned completion from ICH. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO	1b	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Writes to these bit positions have no effect. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the MCH.
6	RO	0b	Reserved
5	RO	0b	**66 MHz Capable:** Does not apply to PCI Express. Hardwired to 0.
4	RO	1b	**Capability List (CLIST):** This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the Capability Identification register resides.
3:0	RO	0000b	Reserved

5.1.5 RID—Revision Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 8h
Default Value: See table below
Access: RO
Size: 8 bits

This register contains the revision number of the MCH Device 0. These bits are read only and writes to this register have no effect.

Bit	Access	Default Value	Description
7:0	RO	see description	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the MCH Device 0. Refer to the *Intel® X48 Express Chipset Specification Update* for the value of this register.

5.1.6 CC—Class Code

B/D/F/Type: 0/0/0/PCI
Address Offset: 9–Bh
Default Value: 060000h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access	Default Value	Description
23:16	RO	06h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the MCH. This code has the value 06h, indicating a Bridge device.
15:8	RO	00h	**Sub-Class Code (SUBCC):** This is an 8-bit value that indicates the category of Bridge into which the MCH falls. The code is 00h indicating a Host Bridge.
7:0	RO	00h	**Programming Interface (PI):** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

5.1.7 MLT—Master Latency Timer

B/D/F/Type: 0/0/0/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

Device 0 in the MCH is not a PCI master. Therefore this register is not implemented.

Bit	Access	Default Value	Description
7:0	RO	00h	Reserved

5.1.8 HDR—Header Type

B/D/F/Type: 0/0/0/PCI
Address Offset: Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access	Default Value	Description
7:0	RO	00h	**PCI Header (HDR):** This field always returns 0 to indicate that the MCH is a single function device with standard header layout. Reads and writes to this location have no effect.

5.1.9 SVID—Subsystem Vendor Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 2C–2Dh
Default Value: 0000h
Access: RWO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Access	Default Value	Description
15:0	RWO	0000h	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

5.1.10 SID—Subsystem Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 2E–2Fh
Default Value: 0000h
Access: RWO
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Access	Default Value	Description
15:0	RWO	0000h	**Subsystem ID (SUBID):** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

5.1.11 CAPPTR—Capabilities Pointer

B/D/F/Type: 0/0/0/PCI
Address Offset: 34h
Default Value: E0h
Access: RO
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Access	Default Value	Description
7:0	RO	E0h	**Capabilities Pointer (CAPPTR):** Pointer to the offset of the first capability ID register block. In this case the first capability is the product-specific Capability Identifier (CAPID0).

5.1.12 PXPEPBAR—PCI Express* Egress Port Base Address

B/D/F/Type: 0/0/0/PCI
Address Offset: 40–47h
Default Value: 0000000000000000h
Access: RO, RW/L
Size: 64 bits

This is the base address for the PCI Express Egress Port MMIO Configuration space. There is no physical memory within this 4 KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the EGRESS port MMIO configuration space is disabled and must be enabled by writing a 1 to PXPEPBAREN [Dev 0, offset 40h, bit 0]

Bit	Access	Default Value	Description
63:36	RO	0000000h	Reserved
35:12	RW/L	000000h	**PCI Express Egress Port MMIO Base Address (PXPEPBAR):** This field corresponds to bits 35 to 12 of the base address PCI Express Egress Port MMIO configuration space. BIOS will program this register resulting in a base address for a 4 KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 64 GB of addressable memory space. System Software uses this base address to program the MCH MMIO register set.
11:1	RO	000h	Reserved
0	RW/L	0b	**PXPEPBAR Enable (PXPEPBAREN):** 0 = PXPEPBAR is disabled and does not claim any memory 1 = PXPEPBAR memory mapped accesses are claimed and decoded appropriately

5.1.13 MCHBAR—MCH Memory Mapped Register Range Base

B/D/F/Type: 0/0/0/PCI
Address Offset: 48–4Fh
Default Value: 0000000000000000h
Access: RO, RW/L
Size: 64 bits

This is the base address for the MCH Memory Mapped Configuration space. There is no physical memory within this 16KB window that can be addressed. The 16 KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the MCH MMIO Memory Mapped Configuration space is disabled and must be enabled by writing a 1 to MCHBAREN [Dev 0, offset48h, bit 0].

The register space contains memory control, initialization, timing, and buffer strength registers; clocking registers; and power and thermal management registers.

Bit	Access	Default Value	Description
63:36	RO	0000000h	Reserved
35:14	RW/L	000000h	**MCH Memory Mapped Base Address (MCHBAR):** This field corresponds to bits 35:14 of the base address MCH Memory Mapped configuration space. BIOS will program this register resulting in a base address for a 16 KB block of contiguous memory address space. This register ensures that a naturally aligned 16 KB space is allocated within the first 64 GB of addressable memory space. System Software uses this base address to program the MCH Memory Mapped register set.
13:1	RO	0000h	Reserved
0	RW/L	0b	**MCHBAR Enable (MCHBAREN):** 0 = MCHBAR is disabled and does not claim any memory 1 = MCHBAR memory mapped accesses are claimed and decoded appropriately

5.1.14 DEVEN—Device Enable

B/D/F/Type: 0/0/0/PCI
Address Offset: 54–57h
Default Value: 000023DBh
Access: RO, RW/L
Size: 32 bits

Allows for enabling/disabling of PCI devices and functions that are within the MCH. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register.

Bit	Access	Default Value	Description
31:14	RO	00000h	Reserved
13	RW/L	1b	**PE1 Enable (D6EN):** 0 = Bus 0, Device 6 is disabled and hidden. 1 = Bus 1, Device 6 is enabled and visible. **NOTE:**
12:11	RO	00b	Reserved
9	RW/L	1b	**EP Function 3 (D3F3EN):** 0 = Bus 0, Device 3, Function 3 is disabled and hidden 1 = Bus 0, Device 3, Function 3 is enabled and visible If Device 3 Function 0 is disabled and hidden, then Device 3 Function 3 is also disabled and hidden independent of the state of this bit. If this MCH does not have ME capability (CAPID0[57] = 1 or CAPID0[56] = 1), then Device 3, Function 3 is disabled and hidden independent of the state of this bit.
8	RW/L	1b	**EP Function 2 (D3F2EN):** 0 = Bus 0, Device 3, Function 2 is disabled and hidden 1 = Bus 0, Device 3, Function 2 is enabled and visible If Device 3 Function 0 is disabled and hidden, then Device 3 Function 2 is also disabled and hidden independent of the state of this bit. If this MCH does not have ME capability (CAPID0[57] = 1 or CAPID0[56] = 1), then Device 3, Function 2 is disabled and hidden independent of the state of this bit.
7	RW/L	1b	**EP Function 1 (D3F1EN):** 0 = Bus 0, Device 3, Function 1 is disabled and hidden 1 = Bus 0, Device 3, Function 1 is enabled and visible. If Device 3 Function 0 is disabled and hidden, then Device 3 Function 1 is also disabled and hidden independent of the state of this bit. If this MCH does not have ME capability (CAPID0[57] = 1), then Device 3, Function 1 is disabled and hidden independent of the state of this bit.
6	RW/L	1b	**EP Function 0 (D3F0EN):** 0 = Bus 0, Device 3, Function 0 is disabled and hidden 1 = Bus 0, Device 3, Function 0 is enabled and visible. If this MCH does not have ME capability (CAPID0[57] = 1), then Device 3, Function 0 is disabled and hidden independent of the state of this bit.

Bit	Access	Default Value	Description
5:2	RO	0s	Reserved
1	RW/L	1b	**PCI Express Port (D1EN):** 0 = Bus 0, Device 1, Function 0 is disabled and hidden. Bus 0, Device 1, Function 0 is enabled and visible.
0	RO	1b	**Host Bridge (D0EN):** Bus 0, Device 0, Function 0 may not be disabled and is therefore hardwired to 1.

5.1.15 PCIEXBAR—PCI Express* Register Range Base Address

B/D/F/Type: 0/0/0/PCI
Address Offset: 60–67h
Default Value: 00000000E0000000h
Access: RO, RW/L, RW/L/K
Size: 64 bits

This is the base address for the PCI Express configuration space. This window of addresses contains the 4 KB of configuration space for each PCI Express device that can potentially be part of the PCI Express Hierarchy associated with the MCH. There is not actual physical memory within this window of up to 256 MB that can be addressed. The actual length is determined by a field in this register. Each PCI Express Hierarchy requires a PCI Express BASE register. The MCH supports one PCI Express hierarchy. The region reserved by this register does not alias to any PCI 2.3 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to the enable field in this register. This base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register), above TOLUD and still within 64 bit addressable memory space. All other bits not decoded are read only 0. The PCI Express Base Address cannot be less than the maximum address written to the Top of physical memory register (TOLUD). Software must guarantee that these ranges do not overlap with known ranges located above TOLUD. Software must ensure that the sum of Length of enhanced configuration region + TOLUD + (other known ranges reserved above TOLUD) is not greater than the 64-bit addressable limit of 64 GB. In general system implementation and number of PCI/PCI express/PCI-X buses supported in the hierarchy will dictate the length of the region.

Bit	Access	Default Value	Description
63:36	RO	0000000h	Reserved
35:28	RW/L	0Eh	**PCI Express Base Address (PCIEXBAR):** This field corresponds to bits [35:28] of the base address for PCI Express enhanced configuration space. BIOS will program this register resulting in a base address for a contiguous memory address space; size is defined by bits [2:1] of this register. This Base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register) above TOLUD and still within 64-bit addressable memory space. The address bits decoded depend on the length of the region defined by this register. The address used to access the PCI Express configuration space for a specific device can be determined as follows: PCI Express Base Address + Bus Number * 1MB + Device Number * 32KB + Function Number * 4KB The address used to access the PCI Express configuration space for Device 1 in this component would be PCI Express Base Address + 0 * 1MB + 1 * 32KB + 0 * 4KB = PCI Express Base Address + 32KB. Remember that this address is the beginning of the 4KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space.
27	RW/L	0b	**128MB Base Address Mask (128ADMSK):** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [2:1] in this register.
26	RW/L	0b	**64MB Base Address Mask (64ADMSK):** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [2:1] in this register.
25:3	RO	000000h	Reserved
2:1	RW/L/K	00b	**Length (LENGTH):** This Field describes the length of this region. Enhanced Configuration Space Region/Buses Decoded 00 = 256 MB (buses 0-255). Bits [31:28] are decoded in the PCI Express Base Address Field 01 = 128 MB (Buses 0–127). Bits [31:27] are decoded in the PCI Express Base Address Field. 10 = 64 MB (Buses 0–63). Bits [31:26] are decoded in the PCI Express Base Address Field. 11 = Reserved
0	RW/L	0b	**PCIEXBAR Enable (PCIEXBAREN):** 0 = The PCIEXBAR register is disabled. Memory read and write transactions proceed as if there were no PCIEXBAR register. PCIEXBAR bits [35:26] are R/W with no functionality behind them. 1 = The PCIEXBAR register is enabled. Memory read and write transactions whose address bits [35:26] match PCIEXBAR will be translated to configuration reads and writes within the MCH. These Translated cycles are routed as shown in the table above.

5.1.16 DMIBAR—Root Complex Register Range Base Address

B/D/F/Type: 0/0/0/PCI
Address Offset: 68–6Fh
Default Value: 0000000000000000h
Access: RO, RW/L
Size: 64 bits

This is the base address for the Root Complex configuration space. This window of addresses contains the Root Complex Register set for the PCI Express Hierarchy associated with the MCH. There is no physical memory within this 4 KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the Root Complex configuration space is disabled and must be enabled by writing a 1 to DMIBAREN [Dev 0, offset 68h, bit 0].

Bit	Access	Default Value	Description
63:36	RO	0000000h	Reserved
35:12	RW/L	000000h	**DMI Base Address (DMIBAR):** This field corresponds to bits 35:12 of the base address DMI configuration space. BIOS will program this register resulting in a base address for a 4 KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 64 GB of addressable memory space. System Software uses this base address to program the DMI register set.
11:1	RO	000h	Reserved
0	RW/L	0b	**DMIBAR Enable (DMIBAREN):** 0 = DMIBAR is disabled and does not claim any memory 1 = DMIBAR memory mapped accesses are claimed and decoded appropriately

5.1.17 PAM0—Programmable Attribute Map 0

B/D/F/Type: 0/0/0/PCI
Address Offset: 90h
Default Value: 00h
Access: RO, RW/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h–0FFFFFh. The MCH allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 768 KB to 1 MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE = 1, the processor read accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI_A.

WE - Write Enable. When WE = 1, the host write accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI_A.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only. Each PAM Register controls two regions, typically 16 KB in size.

Note that the MCH may hang if a PCI Express Link Attach or DMI originated access to Read Disabled or Write Disabled PAM segments occur (due to a possible IWB to non-DRAM).

For these reasons the following critical restriction is placed on the programming of the PAM regions: At the time that a DMI or PCI Express Link Attach accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.

Bit	Access	Default Value	Description
7:6	RO	00b	Reserved
5:4	RW/L	00b	**0F0000–0FFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0F0000h to 0FFFFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:0	RO	0h	Reserved

5.1.18 PAM1—Programmable Attribute Map 1

B/D/F/Type: 0/0/0/PCI
Address Offset: 91h
Default Value: 00h
Access: RO, RW/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h – 0C7FFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	Reserved
5:4	RW/L	00b	**0C4000h–0C7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C4000h to 0C7FFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	Reserved
1:0	RW/L	00b	**0C0000h–0C3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C0000h to 0C3FFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.19 PAM2—Programmable Attribute Map 2

B/D/F/Type: 0/0/0/PCI
Address Offset: 92h
Default Value: 00h
Access: RO, RW/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h– 0CFFFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	Reserved
5:4	RW/L	00b	**0CC000h–0CFFFFh Attribute (HIENABLE):** 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 =: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	Reserved
1:0	RW/L	00b	**0C8000h–0CBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C8000h to 0CBFFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.20 PAM3—Programmable Attribute Map 3

B/D/F/Type: 0/0/0/PCI
Address Offset: 93h
Default Value: 00h
Access: RO, RW/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h – 0D7FFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	Reserved
5:4	RW/L	00b	**0D4000h–0D7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D4000h to 0D7FFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	Reserved
1:0	RW/L	00b	**0D0000h–0D3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D0000h to 0D3FFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.21 PAM4—Programmable Attribute Map 4

B/D/F/Type: 0/0/0/PCI
Address Offset: 94h
Default Value: 00h
Access: RO, RW/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h – 0DFFFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	Reserved
5:4	RW/L	00b	**0DC000h–0DFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0DC000h to 0DFFFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	Reserved
1:0	RW/L	00b	**0D8000h–0DBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D8000h to 0DBFFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.22 PAM5—Programmable Attribute Map 5

B/D/F/Type: 0/0/0/PCI
Address Offset: 95h
Default Value: 00h
Access: RO, RW/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E0000h – 0E7FFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	Reserved
5:4	RW/L	00b	**0E4000h–0E7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000 to 0E7FFF. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	Reserved
1:0	RW/L	00b	**0E0000h–0E3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000 to 0E3FFF. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.23 PAM6—Programmable Attribute Map 6

B/D/F/Type: 0/0/0/PCI
Address Offset: 96h
Default Value: 00h
Access: RO, RW/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h–0EFFFFh.

Bit	Access	Default Value	Description
7:6	RO	00b	Reserved
5:4	RW/L	00b	**0EC000h–0EFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO	00b	Reserved
1:0	RW/L	00b	**0E8000h–0EBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.24 LAC—Legacy Access Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 97h
Default Value: 00h
Access: RW/L, RO
Size: 8 bits

This 8-bit register controls a fixed DRAM hole from 15–16 MB.

Bit	Access	Default Value	Description
7	RW/L	0b	**Hole Enable (HEN):** This field enables a memory hole in DRAM space. The DRAM that lies "behind" this space is not remapped. 0 = No memory hole. 1 = Memory hole from 15 MB to 16 MB.
6:0	RO	0s	Reserved

5.1.25 REMAPBASE—Remap Base Address Register

B/D/F/Type: 0/0/0/PCI
Address Offset: 98–99h
Default Value: 03FFh
Access: RO, RW/L
Size: 16 bits

Bit	Access	Default Value	Description
15:10	RO	000000b	Reserved
9:0	RW/L	3FFh	**Remap Base Address [35:26] (REMAPBASE):** The value in this register defines the lower boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the Remap Base Address are assumed to be 0s. Thus the bottom of the defined memory range will be aligned to a 64 MB boundary. When the value in this register is greater than the value programmed into the Remap Limit register, the Remap window is disabled.

5.1.26 REMAPLIMIT—Remap Limit Address Register

B/D/F/Type: 0/0/0/PCI
Address Offset: 9A–9Bh
Default Value: 0000h
Access: RO, RW/L
Size: 16 bits

Bit	Access	Default Value	Description
15:10	RO	000000b	Reserved
9:0	RW/L	000h	**Remap Limit Address [35:26] (REMAPLMT):** The value in this register defines the upper boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the remap limit address are assumed to be Fs. Thus the top of the defined range will be one less than a 64 MB boundary. When the value in this register is less than the value programmed into the Remap Base register, the Remap window is disabled.

5.1.27 SMRAM—System Management RAM Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 9Dh
Default Value: 02h
Access: RO, RW/L, RW, RW/L/K
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Access	Default Value	Description
7	RO	0b	Reserved
6	RW/L	0b	**SMM Space Open (D_OPEN):** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
5	RW	0b	**SMM Space Closed (D_CLS):** When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
4	RW/L/K	0b	**SMM Space Locked (D_LCK):** When D_LCK is set to 1 then D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	RW/L	0b	**Global SMRAM Enable (G_SMRAME):** If set to a 1, then Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADSB with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes read only.
2:0	RO	010b	**Compatible SMM Space Base Segment (C_BASE_SEG):** This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to DMI. Since the MCH supports only the SMM space between A0000 and BFFFF, this field is hardwired to 010b.

5.1.28 ESMRAMC—Extended System Management RAM Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 9Eh
Default Value: 38h
Access: RW/L, RWC, RO
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bit	Access	Default Value	Description
7	RW/L	0b	**Enable High SMRAM (H_SMRAME):** This bit controls the SMM memory space location (i.e., above 1 MB or below 1 MB) When G_SMRAME is 1 and H_SMRAME is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.
6	RWC	0b	**Invalid SMRAM Access (E_SMERR):** This bit is set when processor has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	RO	1b	**SMRAM Cacheable (SM_CACHE):** This bit is forced to 1 by the MCH.
4	RO	1b	**L1 Cache Enable for SMRAM (SM_L1):** This bit is forced to 1 by the MCH.
3	RO	1b	**L2 Cache Enable for SMRAM (SM_L2):** This bit is forced to 1 by the MCH.
2:1	RW/L	00b	**TSEG Size (TSEG_SZ):** Selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to DMI when the TSEG memory block is enabled. 00 = 1 MB TSEG. (TOLUD – Stolen Memory Size – 1M) to (TOLUD – Stolen Memory Size). 01 = 2 MB TSEG (TOLUD – Stolen Memory Size – 2M) to (TOLUD – Stolen Memory Size). 10 = 8 MB TSEG (TOLUD – Stolen Memory Size – 8M) to (TOLUD – Stolen Memory Size). 11 = Reserved. Once D_LCK has been set, these bits become read only.
0	RW/L	0b	**TSEG Enable (T_EN):** This bit is for enabling of SMRAM memory for Extended SMRAM space only. When G_SMRAME = 1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Note that once D_LCK is set, this bit becomes read only.

5.1.29 TOM—Top of Memory

B/D/F/Type: 0/0/0/PCI
Address Offset: A0–A1h
Default Value: 0001h
Access: RO, RW/L
Size: 16 bits

This Register contains the size of physical memory. BIOS determines the memory size reported to the OS using this Register.

Bit	Access	Default Value	Description
15:10	RO	00h	Reserved
9:0	RW/L	001h	**Top of Memory (TOM):** This register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped IO). These bits correspond to address bits 35:26 (64MB granularity). Bits 25:0 are assumed to be 0.

5.1.30 TOUUD—Top of Upper Usable Dram

B/D/F/Type: 0/0/0/PCI
Address Offset: A2–A3h
Default Value: 0000h
Access: RW/L
Size: 16 bits

This 16 bit register defines the Top of Upper Usable DRAM.

Configuration software must set this value to TOM minus all EP stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit + 1byte 64 MB aligned since reclaim limit is 64 MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4 GB.

Bit	Access	Default Value	Description
15:0	RW/L	0000h	**TOUUD (TOUUD):** This register contains bits 35:20 of an address one byte above the maximum DRAM memory above 4 GB that is usable by the operating system. Configuration software must set this value to TOM minus all EP stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 64 MB aligned since reclaim limit + 1byte is 64 MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4 GB.

5.1.31 BSM—Base of Stolen Memory

B/D/F/Type: 0/0/0/PCI
Address Offset: A4–A7h
Default Value: 00000000h
Access: RW/L, RO
Size: 32 bits

This register contains the base address of stolen DRAM memory. BIOS determines the base of stolen memory by subtracting the stolen memory size (PCI Device 0 offset 52 bits [6:4]) from TOLUD (PCI Device 0 offset B0 bits [15:04]).

Note: This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.

Bit	Access	Default Value	Description
31:20	RW/L	000h	**Base of Stolen Memory (BSM):** This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of stolen memory by subtracting the stolen memory size (PCI Device 0, offset 52h, bits 6:4) from TOLUD (PCI Device 0, offset B0h, bits 15:4). **NOTE:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.
19:0	RO	00000h	Reserved

5.1.32 TSEGMB—TSEG Memory Base

B/D/F/Type: 0/0/0/PCI
Address Offset: AC–AFh
Default Value: 00000000h
Access: RO, RW/L
Size: 32 bits

This register contains the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory by subtracting the TSEG size (PCI Device 0 offset 9E bits [2:1]) from stolen base (PCI Device 0 offset A4 bits [31:20]).

Once D_LCK has been set, these bits becomes read only.

Bit	Access	Default Value	Description
31:20	RW/L	000h	**TESG Memory base (TSEGMB):** This register contains bits [31:20] of the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory by subtracting the TSEG size (PCI Device 0 offset 9E bits [2:1]) from stolen base (PCI Device 0 offset A8 bits [31:20]). Once D_LCK has been set, these bits becomes read only.
19:0	RO	00000h	Reserved

5.1.33 TOLUD—Top of Low Usable DRAM

B/D/F/Type: 0/0/0/PCI
Address Offset: B0–B1h
Default Value: 0010h
Access: RW/L, RO
Size: 16 bits

This 16 bit register defines the Top of Low Usable DRAM. TSEG, and Stolen Memory are within the DRAM space defined. From the top, MCH optionally claims 1, 2 MB of DRAM for Stolen Memory and 1, 2, or 8 MB of DRAM for TSEG if enabled.

Programming Example:

C1DRB3 is set to 4 GB

TSEG is enabled and TSEG size is set to 1 MB

Stolen Memory Size set to 2 MB

BIOS knows the OS requires 1 GB of PCI space.

BIOS also knows the range from FEC0_0000h to FFFF_FFFFh is not usable by the system. This 20 MB range at the very top of addressable memory space is lost to APIC.

According to the above equation, TOLUD is originally calculated to:
4 GB = 1_0000_0000h

The system memory requirements are: 4GB (max addressable space) – 1GB (PCI space) – 35 MB (lost memory) = 3 GB – 35 MB (minimum granularity) = ECB0_0000h

Since ECB0_0000h (PCI and other system requirements) is less than 1_0000_0000h, TOLUD should be programmed to ECBh.

Bit	Access	Default Value	Description
15:4	RW/L	001h	**Top of Low Usable DRAM (TOLUD):** This register contains bits [31:20] of an address one byte above the maximum DRAM memory below 4GB that is usable by the operating system. Address bits [31:20] programmed to 01h implies a minimum memory size of 1 MB. Configuration software must set this value to the smaller of the following 2 choices: maximum amount memory in the system minus ME stolen memory plus one byte or the minimum address allocated for PCI memory. Address bits [19:0] are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. Note that the Top of Low Usable DRAM is the lowest address above both Stolen memory and TSEG. BIOS determines the base of Stolen Memory by subtracting the Stolen Memory Size from TOLUD and further decrements by TSEG size to determine base of TSEG. This register must be 64 MB aligned when reclaim is enabled.
3:0	RO	0000b	Reserved

5.1.34 ERRSTS—Error Status

B/D/F/Type: 0/0/0/PCI
Address Offset: C8–C9h
Default Value: 0000h
Access: RWC/S, RO
Size: 16 bits

This register is used to report various error conditions via the SERR DMI messaging mechanism. An SERR DMI message is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD and PCICMD registers).

These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

Bit	Access	Default Value	Description
15	RO	0b	Reserved
14	RWC/S	0b	**Isochronous TBWRR Run Behind FIFO Full (ITCV):** If set, this bit indicates a VC1 TBWRR is running behind, resulting in the slot timer to stop until the request is able to complete. If this bit is already set, then a interrupt message will not be sent on a new error event.
13	RWC/S	0b	**Isochronous TBWRR Run behind FIFO Put (ITSTV):** If set, this bit indicates a VC1 TBWRR request was put into the run behind. This will likely result in a resulting in a contract violation due to the MCH egress port taking too long to service the isochronous request. If this bit is already set, then a interrupt message will not be sent on a new error event.
12:10	RO	000b	Reserved
9	RWC/S	0b	**LOCK to non-DRAM Memory Flag (LCKF):** When this bit is set to 1, the MCH has detected a lock operation to memory space that did not map into DRAM.
8	RO	0b	Reserved
7	RWC/S	0b	**DRAM Throttle Flag (DTF):** 1 = Indicates that a DRAM Throttling condition occurred. 0 = Software has cleared this flag since the most recent throttling event.
6:2	RO	00h	Reserved
1	RWC/S	0b	**Multiple-bit DRAM ECC Error Flag (DMERR):** If this bit is set to 1, a memory read data transfer had an uncorrectable multiple-bit error. When this bit is set, the address, channel number, and device number that caused the error are logged in the register. Once this bit is set, the fields are locked until the processor clears this bit by writing a 1. Software uses bits [1:0] to detect whether the logged error address is for Single or Multiple-bit error. This bit is reset on PWROK.
0	RWC/S	0b	**Single-bit DRAM ECC Error Flag (DSERR):** If this bit is set to 1, a memory read data transfer had a single-bit correctable error and the corrected data was sent for the access. When this bit is set the address and device number that caused the error are logged in the DEAP register. Once this bit is set the DEAP, DERRSYN, and DERRDST fields are locked to further single bit error updates until the processor clears this bit by writing a 1. A multiple bit error that occurs after this bit is set will overwrite the DEAP and DERRSYN fields with the multiple-bit error signature and the DMERR bit will also be set. A single bit error that occurs after a multi-bit error will set this bit but will not overwrite the other fields. This bit is reset on PWROK.

5.1.35 ERRCMD—Error Command

B/D/F/Type: 0/0/0/PCI
Address Offset: CA–CBh
Default Value: 0000h
Access: RW, RO
Size: 16 bits

This register controls the MCH responses to various system errors. Since the MCH does not have an SERRB signal, SERR messages are passed from the MCH to the ICH over DMI.

When a bit in this register is set, a SERR message will be generated on DMI whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device 0 via the PCI Command register.

Bit	Access	Default Value	Description
15:10	RO	0s	Reserved
9	RW	0b	**SERR on LOCK to non-DRAM Memory (LCKERR):** 1 = The MCH will generate a DMI SERR special cycle whenever a processor lock cycle is detected that does not hit DRAM. 0 = Reporting of this condition via SERR messaging is disabled.
8:2	RO	0s	Reserved
1	RW	0b	**SERR Multiple-Bit DRAM ECC Error (DMERR):** 1 = The MCH generates an SERR message over DMI when it detects a multiple-bit error reported by the DRAM controller. 0 = Reporting of this condition via SERR messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	RW	0b	**SERR on Single-bit ECC Error (DSERR):** 1 = The MCH generates an SERR special cycle over DMI when the DRAM controller detects a single bit error. 0 = Reporting of this condition via SERR messaging is disabled. For systems that do not support ECC this bit must be disabled.

5.1.36 SMICMD—SMI Command

B/D/F/Type: 0/0/0/PCI
Address Offset: CC–CDh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one and only one message type can be enabled.

Bit	Access	Default Value	Description
15:2	RO	0s	Reserved
1	RW	0b	**SMI on Multiple-Bit DRAM ECC Error (DMESMI):** 1 = The MCH generates an SMI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0 = Reporting of this condition via SMI messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	RW	0b	**SMI on Single-bit ECC Error (DSESMI):** 1 = The MCH generates an SMI DMI special cycle when the DRAM controller detects a single bit error. 0 = Reporting of this condition via SMI messaging is disabled. For systems that do not support ECC this bit must be disabled.

5.1.37 SKPD—Scratchpad Data

B/D/F/Type: 0/0/0/PCI
Address Offset: DC–DFh
Default Value: 00000000h
Access: RW
Size: 32 bits

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS drivers.

Bit	Access	Default Value	Description
31:0	RW	0000000 0h	**Scratchpad Data (SKPD):** 1 DWord of data storage.

5.1.38 CAPID0—Capability Identifier

B/D/F/Type: 0/0/0/PCI
Address Offset: E0–EBh
Default Value: 00000000181064000010C0009h
Access: RO
Size: 96 bits
BIOS Optimal Default 0h

This register provides control of bits in this register are only required for customer visible component differentiation.

Bit	Access	Default Value	Description
95:90	RO	0s	Reserved
89	RO	1b	**Chipset Detect:** 0 = Intel X38 Express Chipset 1 = Intel X48 Express Chipset
88:78	RO	0s	Reserved
77	RO	0b	**Dual Channel Disable (DCD):** Disables dual-channel operation 0 = Dual channel operation allowed 1 = Only single channel operation allowed - Only channel 0 will operate, channel 1 will be turned off and tri-stated to save power. This setting hardwires the rank population field for channel 1 to zero. (MCHBAR offset 660h, bits 20:23).
76	RO	0b	**2 DIMMS per Channel Disable (2DPCD):** Allows Dual-Channel operation but only supports 1 DIMM per channel. 0 = 2 DIMMs per channel Enabled 1 = 2 DIMMs per channel disabled. This setting hardwires bits 2 and 3 of the rank population field for each channel to zero. (MCHBAR offset 260h, bits 22:23 for channel 0 and MCHBAR offset 660h, bits 22:23 for channel 1).
75:73	RO	0s	Reserved
72	RO	0b	**Agent Presence Disable (APD):**
71	RO	0b	**Circuit Breaker Disable (CBD):**
70	RO	0b	**Multiprocessor Disable (MD):** 0 = MCH capable of Multiple Processors 1 = MCH capable of uni-processor only.
69	RO	0b	**FAN Speed Control Disable (FSCD):**
68	RO	0b	**EastFork Disable (EFD):**
67:65	RO	000b	Reserved
64:62	RO	110	Reserved
61:58	RO	0000b	Reserved
57	RO	0b	**ME Disable (MED):** 0 = ME feature is enabled 1 = ME feature is disabled
56	RO	1b	Reserved
55:51	RO	0s	Reserved
50:49	RO	11b	Reserved

Bit	Access	Default Value	Description
48	RO	0b	**VT-d Disable (VTDD):** 0 = Enable VT-d 1 = Disable VT-d
47	RO	0b	Reserved
46	RO	1b	Reserved
45	RO	0b	**Primary PCI Express Port x16 Disable (PEX16D):** 0 = Capable of x16 PCI Express Port. 1 = Not Capable of x16 PCI Express port; instead PCI Express is limited to x8 and below. This causes PCI Express port to enable and train logical lanes [7:0] only. Logical lanes [15:8] are powered down, and the Max Link Width field of the Link Capability register reports x8 instead of x16. (In the case of x8 lane reversal, lanes [15:8] are active and lanes [7:0] are powered down.).
44	RO	0b	**Primary PCI Express Port Disable (PEPD):** 0 = There is a PCI Express Port on this MCH. Device 1 and associated memory spaces are accessible. 1 = There is no PCI Express Port on this MCH. Device 1 and associated memory and I/O spaces are disabled by hardwiring the D1EN field bit 1 of the Device Enable register (DEVEN Dev 0 Offset 54h). In addition, Next_Pointer = 00h, and IO cannot decode to the PCI Express interface. From a Physical Layer perspective, all 16 lanes are powered down and the link does not attempt to train.
43	RO	0b	**Secondary PCI Express Port X16 Disable (PE2X16D):** 0 = Capable of x16 PCI Express1 Port. 1 = Not Capable of x16 PCI Express1 port; instead PCI Express1 is limited to x8 and below. This causes PCI Express1 port to enable and train logical lanes [7:0] only. Logical lanes [15:8] are powered down, and the Max Link Width field of the Link Capability register reports x8 instead of x16. (In the case of x8 lane reversal, lanes [15:8] are active and lanes [7:0] are powered down.)
42	RO	0b	**Secondary PCI Express Port Disable (PE2PD):** 0 = There is a secondary PCI Express Port on this MCH. Device 6 and associated memory spaces are accessible. 1 = There is no secondary PCI Express Port on this MCH. Device 6 and associated memory and IO spaces are disabled by hardwiring the D6EN field bit [13] of the Device Enable register (DEVEN Dev 0 Offset 54h). All 16 lanes are powered down and the link does not attempt to train. In addition, Next_Pointer = 00h, and IO cannot decode to the PCI Express interface. From a Physical Layer perspective, all 16 lanes are powered down and the link does not attempt to train.
41	RO	0b	Reserved
40	RO	0b	**ECC Disable (ECCDIS):** 0 = ECC capable 1 = Not ECC capable. Hardwires ECC enable field, bit 7, of the CWB Control Registers (MCHBAR Offset 243h and 643h) to "0".
39	RO	0b	Reserved
38	RO	0b	**DDR3 Disable (DDR3D):** 0 = Capable of supporting DDR3 SDRAM 1 = Not Capable of supporting DDR3 SDRAM
37:35	RO	000b	Reserved

Bit	Access	Default Value	Description
34	RO	0b	**Primary and Secondary PCI Express Gen 2 Disable (PEPSD):** 0 = Primary and secondary PCI Express Gen 2 enabled 1 = Primary and secondary PCI Express Gen 2 disabled
33:32	RO	00b	Reserved
31:30	RO	00b	**DDR Frequency Capability (DDRFC):** This field controls which values may be written to the Memory Frequency Select field [6:4] of the Clocking Configuration registers (MCHBAR Offset C00h). Any attempt to write an unsupported value will be ignored. 00 = MCH capable of "All" Memory Frequencies 01 = MCH capable of up to DDR3 1067 10 = MCH capable of up to DDR3 800 11 = MCH capable of up to DDR3 667
29:28	RO	00b	**FSB Frequency Capability (FSBFC):** This field controls which values are allowed in the FSB Frequency Select Field [2:0] of the Clocking Configuration Register. These values are determined by the BSEL[2:0] frequency straps. Any unsupported strap values will render the MCH System Memory Interface inoperable. 00 = MCH capable of "All" Memory Frequencies 01 = MCH capable of up to FSB 1333 10 = MCH capable of up to FSB 1067 11 = MCH capable of up to FSB 800
27:24	RO	1h	**CAPID Version (CAPIDV):** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO	0Ch	**CAPID Length (CAPIDL):** This field has the value 0Ch to indicate the structure length (12 bytes).
15:8	RO	00h	**Next Capability Pointer (NCP):** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO	09h	**Capability Identifier (CAP_ID):** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

5.2 MCHBAR

Table 10. MCHBAR Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
111h	CHDECMISC	Channel Decode Misc	00h	RW/L
200–201h	C0DRB0	Channel 0 DRAM Rank Boundary Address 0	0000h	RO, RW/L
202–203h	C0DRB1	Channel 0 DRAM Rank Boundary Address 1	0000h	RW/L, RO
204–205h	C0DRB2	Channel 0 DRAM Rank Boundary Address 2	0000h	RW/L, RO
206–207h	C0DRB3	Channel 0 DRAM Rank Boundary Address 3	0000h	RO, RW/L
208–209h	C0DRA01	Channel 0 DRAM Rank 0,1 Attribute	0000h	RW/L
20A	C0DRA23	Channel 0 DRAM Rank 2,3 Attribute	0000h	RW/L
250–251h	C0CYCTRKPCHG	Channel 0 CYCTRK PCHG	0000h	RO, RW
252–255h	C0CYCTRKACT	Channel 0 CYCTRK ACT	00000000h	RW, RO
256–257h	C0CYCTRKWR	Channel 0 CYCTRK WR	0000h	RW
258–25Ah	C0CYCTRKRD	Channel 0 CYCTRK READ	000000h	RO, RW
25B–25Ch	C0CYCTRKREFR	Channel 0 CYCTRK REFR	0000h	RO, RW
260–263h	C0CKECTRL	Channel 0 CKE Control	00000800h	RW, RW/L, RO
269–26Eh	C0REFRCTRL	Channel 0 DRAM Refresh Control	021830000C30h	RW, RO
280–287h	C0ECCERRLOG	Channel 0 ECC Error Log	0000000000000000h	RO/P, RO
29C–29Fh	C0ODTCTRL	Channel 0 ODT Control	00000000h	RO, RW
600–601h	C1DRB0	Channel 1 DRAM Rank Boundary Address 0	0000h	RW/L, RO
602–603h	C1DRB1	Channel 1 DRAM Rank Boundary Address 1	0000h	RO, RW/L
604–605h	C1DRB2	Channel 1 DRAM Rank Boundary Address 2	0000h	RW/L, RO
606–607h	C1DRB3	Channel 1 DRAM Rank Boundary Address 3	0000h	RW/L, RO
608–609h	C1DRA01	Channel 1 DRAM Rank 0,1 Attributes	0000h	RW/L
60A–60Bh	C1DRA23	Channel 1 DRAM Rank 2,3 Attributes	0000h	RW/L
650–651h	C1CYCTRKPCHG	Channel 1 CYCTRK PCHG	0000h	RW, RO
652–655h	C1CYCTRKACT	Channel 1 CYCTRK ACT	00000000h	RO, RW
656–657h	C1CYCTRKWR	Channel 1 CYCTRK WR	0000h	RW

Table 10. MCHBAR Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
658–65Ah	C1CYCTRKRD	Channel 1 CYCTRK READ	000000h	RW, RO
660–663h	C1CKECTRL	Channel 1 CKE Control	00000800h	RO, RW/L, RW
669–66Eh	C1REFRCTRL	Channel 1 DRAM Refresh Control	021830000C 30h	RW, RO
680–687h	C1ECCERRLOG	Channel 1 ECC Error Log	0000000000 000000h	RO/P, RO
69C–69Fh	C1ODTCTRL	Channel 1 ODT Control	00000000h	RO, RW

5.2.1 CHDECMISC—Channel Decode Misc

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 111h
Default Value: 00h
Access: RW/L
Size: 8 bits

This register provides miscellaneous CHDEC/MAGEN configuration bits.

Bit	Access	Default Value	Description
7	RW/L	0b	Reserved
6:5	RW/L	00b	**Enhanced Mode Select (ENHMODESEL):** 00 = Swap Enabled for Bank Selects and Rank Selects 01 = XOR Enabled for Bank Selects and Rank Selects 10 = Swap Enabled for Bank Selects only 11 = XOR Enabled for Bank Select only This register is locked by ME stolen Memory lock.
4	RW/L	0b	**Channel 2 Enhanced Mode (CH2_ENHMODE):**
3	RW/L	0b	**Channel 1 Enhanced Mode (CH1_ENHMODE):**
2	RW/L	0b	**Channel 0 Enhanced Mode (CH0_ENHMODE):**
1	RW/L	0b	Reserved
0	RW/L	0b	**EP Present (EPPRSNT):** This bit indicates whether EP UMA is present in the system or not. This register is locked by ME stolen Memory lock.

5.2.2 C0DRB0—Channel 0 DRAM Rank Boundary Address 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 200–201h
Default Value: 0000h
Access: RO, RW/L
Size: 16 bits

The DRAM Rank Boundary Registers define the upper boundary address of each DRAM rank with a granularity of 64MB. Each rank has its own single-word DRB register. These registers are used to determine which chip select will be active for a given address. Channel and rank map:

ch0 rank0: 200h
ch0 rank1: 202h
ch0 rank2: 204h
ch0 rank3: 206h
ch1 rank0: 600h
ch1 rank1: 602h
ch1 rank2: 604h
ch1 rank3: 606h

Programming Guide:

Non-stacked mode:

If Channel 0 is empty, all of the C0DRBs are programmed with 00h.

C0DRB0 = Total memory in ch0 rank0 (in 64 MB increments)

C0DRB1 = Total memory in ch0 rank0 + ch0 rank1 (in 64 MB increments)

and so on.

If Channel 1 is empty, all of the C1DRBs are programmed with 00h.

C1DRB0 = Total memory in ch1 rank0 (in 64 MB increments)

C1DRB1 = Total memory in ch1 rank0 + ch1 rank1 (in 64 MB increments)

and so on.

Stacked mode:

CODRBs:

Similar to Non-stacked mode.

C1DRB0, C1DRB1 and C1DRB2:

They are also programmed similar to non-stacked mode. Only exception is, the DRBs corresponding to the topmost populated rank and the (unpopulated) higher ranks in Channel 1 must be programmed with the value of the total Channel 1 population plus the value of total Channel 0 population (C0DRB3).

Example: If only ranks 0 and 1 are populated in Ch1 in stacked mode, then

C1DRB0 = Total memory in ch1 rank0 (in 64MB increments)

C1DRB1 = C0DRB3 + Total memory in ch1 rank0 + ch1 rank1 (in 64M B increments) (rank 1 is the topmost populated rank)

C1DRB2 = C1DRB1

C1DRB3 = C1DRB1

C1DRB3:

C1DRB3 = C0DRB3 + Total memory in Channel 1.

Bit	Access	Default Value	Description
15:10	RO	000000b	Reserved
9:0	RW/L	000h	**Channel 0 Dram Rank Boundary Address 0 (C0DRBA0):** This register defines the DRAM rank boundary for rank0 of Channel 0 (64 MB granularity) =R0 R0 = Total rank0 memory size/64MB R1 = Total rank1 memory size/64MB R2 = Total rank2 memory size/64MB R3 = Total rank3 memory size/64MB This register is locked by ME stolen Memory lock.

5.2.3 C0DRB1—Channel 0 DRAM Rank Boundary Address 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 202–203h
Default Value: 0000h
Access: RW/L, RO
Size: 16 bits

See C0DRB0 register.

Bit	Access	Default Value	Description
15:10	RO	000000b	Reserved
9:0	RW/L	000h	**Channel 0 Dram Rank Boundary Address 1 (C0DRBA1):** This field defines the DRAM rank boundary for rank1 of Channel 0 (64 MB granularity) =(R1 + R0) R0 = Total rank0 memory size/64MB R1 = Total rank1 memory size/64MB R2 = Total rank2 memory size/64MB R3 = Total rank3 memory size/64MB This register is locked by ME stolen Memory lock.

5.2.4 C0DRB2—Channel 0 DRAM Rank Boundary Address 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 204–205h
Default Value: 0000h
Access: RW/L, RO
Size: 16 bits

See C0DRB0 register.

Bit	Access	Default Value	Description
15:10	RO	000000b	Reserved
9:0	RW/L	000h	**Channel 0 DRAM Rank Boundary Address 2 (C0DRBA2):** This register defines the DRAM rank boundary for rank2 of Channel 0 (64 MB granularity) =(R2 + R1 + R0) R0 = Total rank0 memory size/64MB R1 = Total rank1 memory size/64MB R2 = Total rank2 memory size/64MB R3 = Total rank3 memory size/64MB This register is locked by ME stolen Memory lock.

5.2.5 C0DRB3—Channel 0 DRAM Rank Boundary Address 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 206–207h
Default Value: 0000h
Access: RO, RW/L
Size: 16 bits

See C0DRB0 register.

Bit	Access	Default Value	Description
15:10	RO	000000b	Reserved
9:0	RW/L	000h	**Channel 0 DRAM Rank Boundary Address 3 (C0DRBA3):** This register defines the DRAM rank boundary for rank3 of Channel 0 (64 MB granularity) =(R3 + R2 + R1 + R0) R0 = Total rank0 memory size/64MB R1 = Total rank1 memory size/64MB R2 = Total rank2 memory size/64MB R3 = Total rank3 memory size/64MB This register is locked by ME stolen Memory lock.

5.2.6 C0DRA01—Channel 0 DRAM Rank 0,1 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 208–209h
Default Value: 0000h
Access: RW/L
Size: 16 bits

The DRAM Rank Attribute Registers define the page sizes/number of banks to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the CxDRA registers describes the page size of a pair of ranks. Channel and rank map:

Ch0 Rank0, 1: 208h–209h

Ch0 Rank2, 3: 20Ah–20Bh

Ch1 Rank0, 1: 608h–609h

Ch1 Rank2, 3: 60Ah–60Bh

DRA[6:0] = "00" means cfg0, DRA[6:0] ="01" means cfg1.... DRA[6:0] = "09" means cfg9 and so on.

DRA[7] indicates whether it's an 8 bank config or not. DRA[7] = 0 means 4 bank, DRA[7] = 1 means 8 bank.

Table 11. DRAM Rank Attribute Register Programming

Config	Tech	DDRx	Depth	Width	Row	Col	Bank	Row Size	Page Size
0	256Mb	2	32M	8	13	10	2	256 MB	8k
1	256Mb	2	16M	16	13	9	2	128 MB	4k
2	512Mb	2	64M	8	14	10	2	512 MB	8k
3	512Mb	2	32M	16	13	10	2	256 MB	8k
4	512Mb	3	64M	8	13	10	3	512 MB	8k
5	512Mb	3	32M	16	12	10	3	256 MB	8k
6	1 Gb	2,3	128M	8	14	10	3	1 GB	8k
7	1 Gb	2,3	64M	16	13	10	3	512 MB	8k

Bit	Access	Default Value	Description
15:8	RW/L	00h	**Channel 0 DRAM Rank-1 Attributes (C0DRA1):** This register defines DRAM pagesize/number-of-banks for rank1 for given channel. See table in register description for programming. This register is locked by ME stolen Memory lock.
7:0	RW/L	00h	**Channel 0 DRAM Rank-0 Attributes (C0DRA0):** This register defines DRAM page size/number-of-banks for rank0 for given channel. See table in register description for programming. This register is locked by ME stolen Memory lock.

5.2.7 C0DRA23—Channel 0 DRAM Rank 2,3 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 20A–20Bh
Default Value: 0000h
Access: RW/L
Size: 16 bits

See C0DRA01 register.

Bit	Access	Default Value	Description
15:8	RW/L	00h	**Channel 0 DRAM Rank-3 Attributes (C0DRA3):** This register defines DRAM pagesize/number-of-banks for rank3 for given channel. See table in register description for programming. This register is locked by ME stolen Memory lock.
7:0	RW/L	00h	**Channel 0 DRAM Rank-2 Attributes (C0DRA2):** This register defines DRAM pagesize/number-of-banks for rank2 for given channel. See table in register description for programming. This register is locked by ME stolen Memory lock.

5.2.8 C0CYCTRKPCHG—Channel 0 CYCTRK PCHG

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 250–251h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This is the Channel 0 CYCTRK Precharge registers.

Bit	Access	Default Value	Description
15:11	RO	00000b	Reserved
10:6	RW	00000b	**Write To PRE Delayed (C0sd_cr_wr_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and PRE commands to the same rank-bank. This field corresponds to t_{WR} in the DDR Specification.
5:2	RW	0000b	**READ To PRE Delayed (C0sd_cr_rd_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and PRE commands to the same rank-bank
1:0	RW	00b	**PRE To PRE Delayed (C0sd_cr_pchg_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between two PRE commands to the same rank.

5.2.9 C0CYCTRKACT—Channel 0 CYCTRK ACT

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 252–255h
Default Value: 00000000h
Access: RW, RO
Size: 32 bits

Channel 0 CYCTRK Activate registers.

Bit	Access	Default Value	Description
31:28	RO	0h	Reserved
27:22	RW	000000b	**ACT Window Count (C0sd_cr_act_windowcnt):** This field indicates the window duration (in DRAM clocks) during which the controller counts the # of activate commands which are launched to a particular rank. If the number of activate commands launched within this window is greater than 4, then a check is implemented to block launch of further activates to this rank for the rest of the duration of this window.
21	RW	0b	**Max ACT Check Disable (C0sd_cr_maxact_dischk):** This field enables the check which ensures that there are no more than four activates to a particular rank in a given window.
20:17	RW	0000b	**ACT to ACT Delayed (C0sd_cr_act_act[]):** This field indicates the minimum allowed spacing (in DRAM clocks) between two ACT commands to the same rank. This field corresponds to t_{RRD} in the DDR Specification.
16:13	RW	0000b	**PRE to ACT Delayed (C0sd_cr_pre_act):** This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE and ACT commands to the same rank-bank:12:9R/W0000bPRE-ALL to ACT Delayed. (C0sd_cr_preall_act):This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and ACT commands to the same rank. This field corresponds to t_{RP} in the DDR Specification.
12:9	RW	0h	**ALLPRE to ACT Delay (C0sd0_cr_preall_act):** From the launch of a prechargeall command wait for these many # of memory clocks before launching a activate command. This field corresponds to t_{PALL_RP} in the DDR Specification.
8:0	RW	000000000b	**REF to ACT Delayed (C0sd_cr_rfsh_act):** This field indicates the minimum allowed spacing (in DRAM clocks) between REF and ACT commands to the same rank. This field corresponds to t_{RFC} in the DDR Specification.

5.2.10 C0CYCTRKWR—Channel 0 CYCTRK WR

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 256–257h
Default Value: 0000h
Access: RW
Size: 16 bits

Channel 0 CYCTRK WR registers.

Bit	Access	Default Value	Description
15:12	RW	0h	**ACT To Write Delay (C0sd_cr_act_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and WRITE commands to the same rank-bank. This field corresponds to t_{RCD_wr} in the DDR Specificaiton.
11:8	RW	0h	**Same Rank Write To Write Delayed (C0sd_cr_wrsr_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to the same rank.
7:4	RW	0h	**Different Rank Write to Write Delay (C0sd_cr_wrdr_wr):** This field register indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to different ranks. This field corresponds to t_{WR_WR} in the DDR Specification.
3:0	RW	0h	**READ To WRTE Delay (C0sd_cr_rd_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and WRITE commands. This field corresponds to t_{RD_WR}.

5.2.11 C0CYCTRKRD—Channel 0 CYCTRK READ

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 258–25Ah
Default Value: 000000h
Access: RO, RW
Size: 24 bits

Channel 0 CYCTRK RD registers.

Bit	Access	Default Value	Description
23:21	RO	000b	Reserved
20:17	RW	0h	**Min ACT To READ Delayed (C0sd_cr_act_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and READ commands to the same rank-bank. This field corresponds to t_{RCD_rd} in the DDR specification.
16:12	RW	00000b	**Same Rank Write To READ Delayed (C0sd_cr_wrsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to the same rank. This field corresponds to t_{WTR} in the DDR specification.
11:8	RW	0000b	**Different Ranks Write To READ Delayed (C0sd_cr_wrdr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to different ranks. This field corresponds to t_{WR_RD} in the DDR specification.
7:4	RW	0000b	**Same Rank Read To Read Delayed (C0sd_cr_rdsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to the same rank.
3:0	RW	0000b	**Different Ranks Read To Read Delayed (C0sd_cr_rddr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to different ranks. This field corresponds to t_{RD_RD}.

5.2.12 C0CYCTRKREFR—Channel 0 CYCTRK REFR

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 25B–25Ch
Default Value: 0000h
Access: RO, RW
Size: 16 bits

Channel 0 CYCTRK Refresh registers.

Bit	Access	Default Value	Description
15:13	RO	000b	Reserved
12:9	RW	0000b	**Same Rank PALL to REF Delayed (C0sd_cr_pchgall_rfsh):** This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and REF commands to the same rank.
8:0	RW	000000000b	**Same Rank REF to REF Delayed (C0sd_cr_rfsh_rfsh):** This field indicates the minimum allowed spacing (in DRAM clocks) between two REF commands to same ranks.

5.2.13 C0CKECTRL—Channel 0 CKE Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 260–263h
Default Value: 00000800h
Access: RW, RW/L, RO
Size: 32 bits

This register provides CKE controls for Channel 0.

Bit	Access	Default Value	Description
31:28	RO	0000b	Reserved
27	RW	0b	**Start the Self-Refresh Exit Sequence (sd0_cr_srcstart):** This field indicates the request to start the self-refresh exit sequence
26:24	RW	000b	**CKE Pulse Width Requirement in High Phase (sd0_cr_cke_pw_hl_safe):** This field indicates CKE pulse width requirement in high phase. This field corresponds to t_{CKE} (high) in the DDR specification.
23	RW/L	0b	**Rank 3 Population (sd0_cr_rankpop3):** 1 = Rank 3 populated 0 = Rank 3 not populated This register is locked by ME stolen Memory lock.
22	RW/L	0b	**Rank 2 Population (sd0_cr_rankpop2):** 1 = Rank 2 populated 0 = Rank 2 not populated This register is locked by ME stolen Memory lock.
21	RW/L	0b	**Rank 1 Population (sd0_cr_rankpop1):** 1 = Rank 1 populated 0 = Rank 1 not populated This register is locked by ME stolen Memory lock.
20	RW/L	0b	**Rank 0 Population (sd0_cr_rankpop0):** 1 = Rank 0 populated 0 = Rank 0 not populated This register is locked by ME stolen Memory lock.
19:17	RW	000b	**CKE Pulse Width Requirement in Low Phase (sd0_cr_cke_pw_lh_safe):** This configuration register indicates CKE pulse width requirement in low phase. This field corresponds to t_{CKE} (low) in the DDR specification.
16	RW	0b	**Enable CKE Toggle for PDN Entry/Exit (sd0_cr_pdn_enable):** This bit indicates that the toggling of CKEs (for PDN entry/exit) is enabled.
15:14	RO	00b	Reserved
13:10	RW	0010b	**Minimum Powerdown exit to Non-Read command spacing (sd0_cr_txp):** This field indicates the minimum number of clocks to wait following assertion of CKE before issuing a non-read command. 1010–1111 = Reserved. 0010–1001 = 2–9clocks. 0000–0001 = Reserved.
9:1	RW	000000000b	**Self Refresh Exit Count (sd0_cr_slfrfsh_exit_cnt):** This field indicates the Self refresh exit count. (Program to 255). This field corresponds to t_{XSNR}/t_{XSRD} in the DDR Specification.
0	RW	0b	**Indicates only 1 DIMM Populated (sd0_cr_singledimmpop):** This field indicates the that only 1 DIMM is populated.

5.2.14 C0REFRCTRL—Channel 0 DRAM Refresh Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 269–26Eh
Default Value: 021830000C30h
Access: RW, RO
Size: 48 bits

Settings to configure the DRAM refresh controller.

Bit	Access	Default Value	Description
47:42	RO	00h	Reserved
41:37	RW	10000b	**Direct Rcomp Quiet Window (DIRQUIET):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
36:32	RW	11000b	**Indirect Rcomp Quiet Window (INDIRQUIET):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
31:27	RW	00110b	**Rcomp Wait (RCOMPWAIT):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
26	RW	0b	Reserved
25	RW	0b	**Refresh Counter Enable (REFCNTEN):** This bit is used to enable the refresh counter to count during times that DRAM is not in self-refresh, but refreshes are not enabled. Such a condition may occur due to need to reprogram DIMMs following DRAM controller switch. This bit has no effect when Refresh is enabled (i.e. there is no mode where Refresh is enabled but the counter does not run) So, in conjunction with bit [23] REFEN, the modes are: **[REFEN:REFCNTEN] Description** [0:0] Normal refresh disable [0:1] Refresh disabled, but counter is accumulating refreshes. [1:X] Normal refresh enable
24	RW	0b	**All Rank Refresh (ALLRKREF):** This configuration bit enables (by default) that all the ranks are refreshed in a staggered/atomic fashion. If set, the ranks are refreshed in an independent fashion.
23	RW	0b	**Refresh Enable (REFEN):** Refresh is enabled. 0 = Disabled 1 = Enabled
22	RW	0b	**DDR Initialization Done (INITDONE):** Indicates that DDR initialization is complete.
21:20	RW	00b	Reserved
19:18	RW	00b	**DRAM Refresh Panic Watermark (REFPANICWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_panic flag is set. 00 = 5 01 = 6 10 = 7 11 = 8

Bit	Access	Default Value	Description
17:16	RW	00b	**DRAM Refresh High Watermark (REFHIGHWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_high flag is set. 00 = 3 01 = 4 10 = 5 11 = 6
15:14	RW	00b	**DRAM Refresh Low Watermark (REFLOWWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_low flag is set. 00 = 1 01 = 2 10 = 3 11 = 4
13:0	RW	00110000 110000b	**Refresh Counter Time Out Value (REFTIMEOUT):** Program this field with a value that will provide 7.8 us at the memory clock frequency. At various memory clock frequencies, this results in the following values: 400 Mhz -> C30 hex (Default Value) 533 Mhz -> 104B hex 666 Mhz -> 1450 hex

5.2.15 C0ECCERRLOG—Channel 0 ECC Error Log

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 280–287h
Default Value: 0000000000000000h
Access: RO/P, RO
Size: 64 bits

This register is used to store the error status information in ECC enabled configurations, along with the error syndrome and the rank/bank/row/column address information of the address block of main memory of which an error (single bit or multi-bit error) has occurred. Note that the address fields represent the address of the first single or the first multiple bit error occurrence after the error flag bits in the ERRSTS register have been cleared by software. A multiple bit error will overwrite a single bit error. Once the error flag bits are set as a result of an error, this bit field is locked and doesn't change as a result of a new error until the error flag is cleared by software. Same is the case with error syndrome field, but the following priority needs to be followed if more than one error occurs on one or more of the 4 QWs. MERR on QW0 MERR on QW1 MERR on QW2 MERR on QW3 CERR on QW0 CERR on QW1 CERR on QW2 CERR on QW3

Bit	Access	Default Value	Description
63:48	RO/P	0000h	**Error Column Address (ERRCOL):** Row address of the address block of main memory of which an error (single bit or multi-bit error) has occurred.
47:32	RO/P	0000h	**Error Row Address (ERRROW):** Row address of the address block of main memory of which an error (single bit or multi-bit error) has occurred.
31:29	RO/P	000b	**Error Bank Address (ERRBANK):** Rank address of the address block of main memory of which an error (single bit or multi-bit error) has occurred.
28:27	RO/P	00b	**Error Rank Address (ERRRANK):** Rank address of the address block of main memory of which an error (single bit or multi-bit error) has occurred. 00 = rank 0 (DIMM0) 01 = rank 1 (DIMM0) 10 = rank 2 (DIMM1) 11 = rank 3 (DIMM1)
26:24	RO	0h	Reserved
23:16	RO/P	00h	**Error Syndrome (ERRSYND):** Syndrome that describes the set of bits associated with the first failing quadword.
15:2	RO	0h	Reserved
1	RO/P	0b	**Multiple Bit Error Status (MERRSTS):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked until this bit is cleared. This bit is cleared when it receives an indication that the processor has cleared the corresponding bit in the ERRSTS register.
0	RO/P	0b	**Correctable Error Status (CERRSTS):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. But, a multiple bit error that occurs after this bit is set will over-write the address/error syndrome info. This bit is cleared when it receives an indication that the processor has cleared the corresponding bit in the ERRSTS register.

5.2.16 C0ODTCTRL—Channel 0 ODT Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 29C–29Fh
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

This register provides ODT controls.

Bit	Access	Default Value	Description
31:12	RO	00000h	Reserved
11:8	RW	0h	**DRAM ODT for Read Commands (sd0_cr_odt_duration_rd):** Specifies the duration in MDCLKs to assert DRAM ODT for Read Commands. The Async value should be used when the Dynamic Powerdown bit is set. Else use the Sync value.
7:4	RW	0h	**DRAM ODT for Write Commands (sd0_cr_odt_duration_wr):** Specifies the duration in MDCLKs to assert DRAM ODT for Write Commands. The Async value should be used when the Dynamic Powerdown bit is set. Else use the Sync value.
3:0	RW	0h	**MCH ODT for Read Commands (sd0_cr_mchodt_duration):** Specifies the duration in MDCLKs to assert MCH ODT for Read Commands

5.2.17 C1DRB0—Channel 1 DRAM Rank Boundary Address 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 600–601h
Default Value: 0000h
Access: RW/L, RO
Size: 16 bits

The operation of this register is detailed in the description for the C0DRB0 register.

Bit	Access	Default Value	Description
15:10	RO	000000b	Reserved
9:0	RW/L	000h	**Channel 1 DRAM Rank Boundary Address 0 (C1DRBA0):** See C0DRB0 register. In stacked mode, if this is the topmost populated rank in Channel 1, program this value to be cumulative of Ch0 DRB3. This register is locked by ME stolen Memory lock.

5.2.18 C1DRB1—Channel 1 DRAM Rank Boundary Address 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 602–603h
Default Value: 0000h
Access: RO, RW/L
Size: 16 bits

The operation of this register is detailed in the description for the C0DRB0 register.

Bit	Access	Default Value	Description
15:10	RO	000000b	Reserved
9:0	RW/L	000h	**Channel 1 DRAM Rank Boundary Address 1 (C1DRBA1):** See C0DRB1 register. In stacked mode, if this is the topmost populated rank in Channel 1, program this value to be cumulative of Ch0 DRB3. This register is locked by ME stolen Memory lock.

5.2.19 C1DRB2—Channel 1 DRAM Rank Boundary Address 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 604–605h
Default Value: 0000h
Access: RW/L, RO
Size: 16 bits

The operation of this register is detailed in the description for the C0DRB0 register.

Bit	Access	Default Value	Description
15:10	RO	000000b	Reserved
9:0	RW/L	000h	**Channel 1 DRAM Rank Boundary Address 2 (C1DRBA2):** See C0DRB2 register. In stacked mode, if this is the topmost populated rank in Channel 1, program this value to be cumulative of Ch0 DRB3. This register is locked by ME stolen Memory lock.

5.2.20 C1DRB3—Channel 1 DRAM Rank Boundary Address 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 606–607h
Default Value: 0000h
Access: RW/L, RO
Size: 16 bits

The operation of this register is detailed in the description for the C0DRB0 register.

Bit	Access	Default Value	Description
15:10	RO	000000b	Reserved
9:0	RW/L	000h	**Channel 1 DRAM Rank Boundary Address 3 (C1DRBA3):** See C0DRB3 register. In stacked mode, this will be cumulative of Ch0 DRB3. This register is locked by ME stolen Memory lock.

5.2.21 C1DRA01—Channel 1 DRAM Rank 0,1 Attributes

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 608–609h
Default Value: 0000h
Access: RW/L
Size: 16 bits

The operation of this register is detailed in the description for register C0DRA01.

Bit	Access	Default Value	Description
15:8	RW/L	00h	**Channel 1 DRAM Rank-1 Attributes (C1DRA1):** See C0DRA1 register. This register is locked by ME stolen Memory lock.
7:0	RW/L	00h	**Channel 1 DRAM Rank-0 Attributes (C1DRA0):** See C0DRA0 register. This register is locked by ME stolen Memory lock.

5.2.22 C1DRA23—Channel 1 DRAM Rank 2,3 Attributes

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 60A–60Bh
Default Value: 0000h
Access: RW/L
Size: 16 bits

The operation of this register is detailed in the description for the C0DRA01 register.

Bit	Access	Default Value	Description
15:8	RW/L	00h	**Channel 1 DRAM Rank-3 Attributes (C1DRA3):** See C0DRA3 register. This register is locked by ME stolen Memory lock.
7:0	RW/L	00h	**Channel 1 DRAM Rank-2 Attributes (C1DRA2):** See C0DRA2 register. This register is locked by ME stolen Memory lock.

5.2.23 C1CYCTRKPCHG—Channel 1 CYCTRK PCHG

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 650–651h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

Channel 1 CYCTRK Precharge registers.

Bit	Access	Default Value	Description
15:11	RO	00000b	Reserved
10:6	RW	00000b	**Write To PRE Delayed (C1sd_cr_wr_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and PRE commands to the same rank-bank. This field corresponds to t_{WR} in the DDR Specification.
5:2	RW	0000b	**READ To PRE Delayed (C1sd_cr_rd_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and PRE commands to the same rank-bank
1:0	RW	00b	**PRE To PRE Delayed (C1sd_cr_pchg_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between two PRE commands to the same rank.

5.2.24 C1CYCTRKACT—Channel 1 CYCTRK ACT

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 652–655h
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

Channel 1 CYCTRK ACT registers.

Bit	Access	Default Value	Description
31:28	RO	0h	Reserved
27:22	RW	000000b	**ACT Window Count (C1sd_cr_act_windowcnt):** This field indicates the window duration (in DRAM clocks) during which the controller counts the # of activate commands which are launched to a particular rank. If the number of activate commands launched within this window is greater than 4, then a check is implemented to block launch of further activates to this rank for the rest of the duration of this window.
21	RW	0b	**Max ACT Check Disable (C1sd_cr_maxact_dischk):**This field enables the check which ensures that there are no more than four activates to a particular rank in a given window.
20:17	RW	0000b	**ACT to ACT Delayed (C1sd_cr_act_act[]):** This field indicates the minimum allowed spacing (in DRAM clocks) between two ACT commands to the same rank. This field corresponds to t_{RRD} in the DDR specification.

Bit	Access	Default Value	Description
16:13	RW	0000b	**PRE to ACT Delayed (C1sd_cr_pre_act):** This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE and ACT commands to the same rank-bank:12:9R/W0000bPRE-ALL to ACT Delayed (C1sd_cr_preall_act):This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and ACT commands to the same rank. This field corresponds to t_{RP} in the DDR Specification.
12:9	RW	0h	**ALLPRE to ACT Delay (C1sd_cr_preall_act):** From the launch of a prechargeall command wait for these many # of memory clocks before launching a activate command. This field corresponds to t_{PALL_RP}.
8:0	RW	000000000b	**REF to ACT Delayed (C1sd_cr_rfsh_act):** This field indicates the minimum allowed spacing (in DRAM clocks) between REF and ACT commands to the same rank. This field corresponds to t_{RFC} in the DDR specification.

5.2.25 C1CYCTRKWR—Channel 1 CYCTRK WR

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 656–657h
Default Value: 0000h
Access: RW
Size: 16 bits

Channel 1 CYCTRK WR registers.

Bit	Access	Default Value	Description
15:12	RW	0h	**ACT To Write Delay (C1sd_cr_act_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and WRITE commands to the same rank-bank. This field corresponds to t_{RCD_wr} in the DDR Specification.
11:8	RW	0h	**Same Rank Write To Write Delayed (C1sd_cr_wrsr_wr):** This field register indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to the same rank.
7:4	RW	0h	**Different Rank Write to Write Delay (C1sd_cr_wrdr_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to different ranks. This field corresponds to t_{WR_WR} in the DDR Specification.
3:0	RW	0h	**READ To WRTE Delay (C1sd_cr_rd_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and WRITE commands. This field corresponds to t_{RD_WR}.

5.2.26 C1CYCTRKRD—Channel 1 CYCTRK READ

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 658–65Ah
Default Value: 000000h
Access: RW, RO
Size: 24 bits

Channel 1 CYCTRK READ registers.

Bit	Access	Default Value	Description
23:21	RO	0h	Reserved
20:17	RW	0h	**Min ACT To READ Delayed (C1sd_cr_act_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and READ commands to the same rank-bank. This field Corresponds to t_{RCD_rd} in the DDR Specification
16:12	RW	00000b	**Same Rank Write To READ Delayed (C1sd_cr_wrsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to the same rank. This field corresponds to t_{WTR} in the DDR Specification.
11:8	RW	0000b	**Different Ranks Write To READ Delayed (C1sd_cr_wrdr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to different ranks. This field corresponds to t_{WR_RD} in the DDR Specification.
7:4	RW	0000b	**Same Rank Read To Read Delayed (C1sd_cr_rdsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to the same rank.
3:0	RW	0000b	**Different Ranks Read To Read Delayed (C1sd_cr_rddr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to different ranks. This field corresponds to t_{RD_RD}.

5.2.27 C1CKECTRL—Channel 1 CKE Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 660–663h
Default Value: 00000800h
Access: RO, RW/L, RW
Size: 32 bits

Channel 1 CKE Control registers.

Bit	Access	Default Value	Description
31:28	RO	0h	Reserved
27	RW	0b	**Start the Self-Refresh Exit Sequence (sd1_cr_srcstart):** This bit indicates the request to start the self-refresh exit sequence
26:24	RW	000b	**CKE Pulse Width Requirement in High Phase (sd1_cr_cke_pw_hl_safe):** This bit indicates CKE pulse width requirement in high phase. This field Corresponds to t_{CKE} (high) in the DDR Specification.
23	RW/L	0b	**Rank 3 Population (sd1_cr_rankpop3):** 1 = Rank 3 populated 0 = Rank 3 not populated This register is locked by ME stolen Memory lock.
22	RW/L	0b	**Rank 2 Population (sd1_cr_rankpop2):** 1 = Rank 2 populated 0 = Rank 2 not populated This register is locked by ME stolen Memory lock.
21	RW/L	0b	**Rank 1 Population (sd1_cr_rankpop1):** 1 = Rank 1 populated 0 = Rank 1 not populated This register is locked by ME stolen Memory lock.
20	RW/L	0b	**Rank 0 Population (sd1_cr_rankpop0):** 1 = Rank 0 populated 0 = Rank 0 not populated This register is locked by ME stolen Memory lock.
19:17	RW	000b	**CKE Pulse Width Requirement in Low Phase (sd1_cr_cke_pw_lh_safe):** This field indicates CKE pulse width requirement in low phase. This field Corresponds to t_{CKE} (low) in the DDR Specification.
16	RW	0b	**Enable CKE Toggle for PDN Entry/Exit (sd1_cr_pdn_enable):** This bit indicates that the toggling of CKEs (for PDN entry/exit) is enabled.
15:14	RO	00b	Reserved
13:10	RW	0010b	**Minimum Powerdown Exit to Non-Read Command Spacing (sd1_cr_txp):** This field indicates the minimum number of clocks to wait following assertion of CKE before issuing a non-read command. 1010–1111 = Reserved. 0010–1001 = 2–9 clocks 0000–0001 = Reserved.
9:1	RW	0000000 00b	**Self Refresh Exit Count (sd1_cr_slfrfsh_exit_cnt):** This configuration register indicates the Self refresh exit count. (Program to 255) Corresponds to t_{XSNR}/t_{XSRD} in the DDR Specification.
0	RW	0b	**Indicates Only 1 DIMM Populated (sd1_cr_singledimmpop):** This field indicates the that only 1 DIMM is populated.

5.2.28 C1REFRCTRL—Channel 1 DRAM Refresh Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 669–66Eh
Default Value: 021830000C30h
Access: RW, RO
Size: 48 bits

Settings to configure the DRAM refresh controller.

Bit	Access	Default Value	Description
47:42	RO	00h	Reserved
41:37	RW	10000b	**Direct Rcomp Quiet Window (DIRQUIET):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
36:32	RW	11000b	**Indirect Rcomp Quiet Window (INDIRQUIET):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
31:27	RW	00110b	**Rcomp Wait (RCOMPWAIT):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
26	RO	0b	Reserved
25	RW	0b	**Refresh Counter Enable (REFCNTEN):** This bit is used to enable the refresh counter to count during times that DRAM is not in self-refresh, but refreshes are not enabled. Such a condition may occur due to need to reprogram DIMMs following DRAM controller switch. This bit has no effect when Refresh is enabled (i.e. there is no mode where Refresh is enabled but the counter does not run) So, in conjunction with bit 23 REFEN, the modes are: **[REFEN:REFCNTEN]Description** [0:0] Normal refresh disable [0:1] Refresh disabled, but counter is accumulating refreshes. [1:X] Normal refresh enable
24	RW	0b	**All Rank Refresh (ALLRKREF):** This configuration bit enables (by default) that all the ranks are refreshed in a staggered/atomic fashion. If set, the ranks are refreshed in an independent fashion.
23	RW	0b	**Refresh Enable (REFEN):** Refresh is enabled. 0 = Disabled 1 = Enabled
22	RW	0b	**DDR Initialization Done (INITDONE):** Indicates that DDR initialization is complete.
21:20	RO	00b	Reserved
19:18	RW	00b	**DRAM Refresh Panic Watermark (REFPANICWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_panic flag is set. 00 = 5 01 = 6 10 = 7 11 = 8

Bit	Access	Default Value	Description
17:16	RW	00b	**DRAM Refresh High Watermark (REFHIGHWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_high flag is set. 00 = 3 01 = 4 10 = 5 11 = 6
15:14	RW	00b	**DRAM Refresh Low Watermark (REFLOWWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_low flag is set. 00 = 1 01 = 2 10 = 3 11 = 4
13:0	RW	0011000 0110000 b	**Refresh Counter Time Out Value (REFTIMEOUT):** Program this field with a value that will provide 7.8 us at the memory clock frequency. At various memory clock frequencies, this results in the following values: 400 Mhz -> C30 hex (Default Value) 533 Mhz -> 104B hex 666 Mhz -> 1450 hex

5.2.29 C1ECCERRLOG—Channel 1 ECC Error Log

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 680–687h
Default Value: 0000000000000000h
Access: RO/P, RO
Size: 64 bits

This register is used to store the error status information in ECC enabled configurations, along with the error syndrome and the rank/bank/row/column address information of the address block of main memory of which an error (single bit or multi-bit error) has occurred. Note that the address fields represent the address of the first single or the first multiple bit error occurrence after the error flag bits in the ERRSTS register have been cleared by software. A multiple bit error will overwrite a single bit error. Once the error flag bits are set as a result of an error, this bit field is locked and does not change as a result of a new error until the error flag is cleared by software. Same is the case with error syndrome field, but the following priority needs to be followed if more than one error occurs on one or more of the 4 QWs. MERR on QW0, MERR on QW1, MERR on QW2, MERR on QW3, CERR on QW0, CERR on QW1, CERR on QW2, CERR on QW3.

Bit	Access	Default Value	Description
63:48	RO/P	0000h	**Error Column Address (ERRCOL):** Row address of the address block of main memory of which an error (single bit or multi-bit error) has occurred.
47:32	RO/P	0000h	**Error Row Address (ERRROW):** Row address of the address block of main memory of which an error (single bit or multi-bit error) has occurred.
31:29	RO/P	000b	**Error Bank Address (ERRBANK):** Rank address of the address block of main memory of which an error (single bit or multi-bit error) has occurred.

Bit	Access	Default Value	Description
28:27	RO/P	00b	**Error Rank Address (ERRRANK):** Rank address of the address block of main memory of which an error (single bit or multi-bit error) has occurred. 00 = rank 0 (DIMM0) 01 = rank 1 (DIMM0) 10 = rank 2 (DIMM1) 11 = rank 3 (DIMM1)
26:24	RO	0h	Reserved
23:16	RO/P	00h	**Error Syndrome (ERRSYND):** Syndrome that describes the set of bits associated with the first failing quadword.
15:2	RO	0h	Reserved
1	RO/P	0b	**Multiple Bit Error Status (MERRSTS):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked until this bit is cleared. This bit is cleared when it receives an indication that the processor has cleared the corresponding bit in the ERRSTS register.
0	RO/P	0b	**Correctable Error Status (CERRSTS):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. But, a multiple bit error that occurs after this bit is set will over-write the address/error syndrome info. This bit is cleared when it receives an indication that the processor has cleared the corresponding bit in the ERRSTS register.

5.2.30 C1ODTCTRL—Channel 1 ODT Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 69C–69Fh
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

This register provides ODT controls.

Bit	Access	Default Value	Description
31:12	RO	00000h	Reserved
11:8	RW	0h	**DRAM ODT for Read Commands (sd1_cr_odt_duration_rd):** Specifies the duration in MDCLKs to assert DRAM ODT for Read Commands. The Async value should be used when the Dynamic Powerdown bit is set. Else use the Sync value.
7:4	RW	0h	**DRAM ODT for Write Commands (sd1_cr_odt_duration_wr):** Specifies the duration in MDCLKs to assert DRAM ODT for Write Commands. The Async value should be used when the Dynamic Powerdown bit is set. Else use the Sync value.
3:0	RW	0h	**MCH ODT for Read Commands (sd1_cr_mchodt_duration):** Specifies the duration in MDCLKs to assert MCH ODT for Read Commands.

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6 Host-Primary PCI Express* Bridge Registers (D1:F0)

Device 1 contains the controls associated with the PCI Express root port that is the intended attach point for external devices. In addition, it also functions as the virtual PCI-to-PCI bridge. The table below provides an address map of the D1:F0 registers listed by address offset in ascending order. This chapter provides a detailed bit description of the registers.

Warning: When reading the PCI Express "conceptual" registers such as this, you may not get a valid value unless the register value is stable.

The *PCI Express* Specification* defines two types of reserved bits:

Reserved and Preserved:

- Reserved for future RW implementations; software must preserve value read for writes to bits.
- Reserved and Zero: Reserved for future R/WC/S implementations; software must use 0 for writes to bits.

Unless explicitly documented as Reserved and Zero, all bits marked as reserved are part of the Reserved and Preserved type, which have historically been the typical definition for Reserved.

Note: Most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first disable the link, then program the registers, and then re-enable the link (which will cause a full-retrain with the new settings).

Table 12. Host-PCI Express Bridge Register Address Map (D1:F0) (Sheet 1 of 3)

Address Offset	Register Symbol	Register Name	Default Value	Access
0–1h	VID1	Vendor Identification	8086h	RO
2–3h	DID1	Device Identification	29E1h	RO
4–5h	PCICMD1	PCI Command	0000h	RO, RW
6–7h	PCISTS1	PCI Status	0010h	RO, RWC
8h	RID1	Revision Identification	see register description	RO
9–Bh	CC1	Class Code	060400h	RO
Ch	CL1	Cache Line Size	00h	RW
Eh	HDR1	Header Type	01h	RO
18h	PBUSN1	Primary Bus Number	00h	RO
19h	SBUSN1	Secondary Bus Number	00h	RW
1Ah	SUBUSN1	Subordinate Bus Number	00h	RW
1Ch	IOBASE1	I/O Base Address	F0h	RO, RW
1Dh	IOLIMIT1	I/O Limit Address	00h	RW, RO
1E–1Fh	SSTS1	Secondary Status	0000h	RO, RWC

Table 12. Host-PCI Express Bridge Register Address Map (D1:F0) (Sheet 2 of 3)

Address Offset	Register Symbol	Register Name	Default Value	Access
20–21h	MBASE1	Memory Base Address	FFF0h	RW, RO
22–23h	MLIMIT1	Memory Limit Address	0000h	RW, RO
24–25h	PMBASE1	Prefetchable Memory Base Address	FFF1h	RW, RO
26–27h	PMLIMIT1	Prefetchable Memory Limit Address	0001h	RO, RW
28–2Bh	PMBASEU1	Prefetchable Memory Base Address Upper	00000000h	RW
2C–2Fh	PMLIMITU1	Prefetchable Memory Limit Address Upper	00000000h	RW
34h	CAPPTR1	Capabilities Pointer	88h	RO
3Ch	INTRLINE1	Interrupt Line	00h	RW
3Dh	INTRPIN1	Interrupt Pin	01h	RO
3E–3Fh	BCTRL1	Bridge Control	0000h	RO, RW
80–83h	PM_CAPID1	Power Management Capabilities	C8039001h	RO
84–87h	PM_CS1	Power Management Control/Status	00000008h	RO, RW, RW/P
88–8Bh	SS_CAPID	Subsystem ID and Vendor ID Capabilities	0000800Dh	RO
8C–8Fh	SS	Subsystem ID and Subsystem Vendor ID	00008086h	RWO
90–91h	MSI_CAPID	Message Signaled Interrupts Capability ID	A005h	RO
92–93h	MC	Message Control	0000h	RW, RO
94–97h	MA	Message Address	00000000h	RO, RW
98–99h	MD	Message Data	0000h	RW
A0–A1h	PE_CAPL	PCI Express Capability List	0010h	RO
A2–A3h	PE_CAP	PCI Express Capabilities	0142h	RO, RWO
A4–A7h	DCAP	Device Capabilities	00008000h	RO
A8–A9h	DCTL	Device Control	0000h	RW, RO
AA–ABh	DSTS	Device Status	0000h	RO, RWC
AC–AFh	LCAP	Link Capabilities	020214D02h	RO, RWO
B0–B1h	LCTL	Link Control	0000h	RO, RW, RW/SC
B2–B3h	LSTS	Link Status	1000h	RWC, RO
B4–B7h	SLOTCAP	Slot Capabilities	00040000h	RWO, RO
B8–B9h	SLOTCTL	Slot Control	0000h	RO, RW
BA–BBh	SLOTSTS	Slot Status	0000h	RO, RWC
BC–BDh	RCTL	Root Control	0000h	RO, RW
C0–C3h	RSTS	Root Status	00000000h	RO, RWC
EC–EFh	PELC	PCI Express Legacy Control	00000000h	RO, RW
100–103h	VCECH	Virtual Channel Enhanced Capability Header	14010002h	RO
104–107h	PVCCAP1	Port VC Capability Register 1	00000000h	RO

Table 12. Host-PCI Express Bridge Register Address Map (D1:F0) (Sheet 3 of 3)

Address Offset	Register Symbol	Register Name	Default Value	Access
108–10Bh	PVCCAP2	Port VC Capability Register 2	00000000h	RO
10C–10Dh	PVCCTL	Port VC Control	0000h	RO, RW
110–113h	VC0RCAP	VC0 Resource Capability	00000001h	RO
114–117h	VC0RCTL	VC0 Resource Control	800000FFh	RO, RW
11A–11Bh	VC0RSTS	VC0 Resource Status	0002h	RO
140–143h	RCLDECH	Root Complex Link Declaration Enhanced	00010005h	RO
144–147h	ESD	Element Self Description	02000100h	RO, RWO
150–153h	LE1D	Link Entry 1 Description	00000000h	RO, RWO
158–15Fh	LE1A	Link Entry 1 Address	0000000000000000h	RO, RWO
218–21Fh	PESSTS	PCI Express Sequence Status	0000000000000FFFh	RO

6.1 VID1—Vendor Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 0–1h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identify any PCI device.

Bit	Access	Default Value	Description
15:0	RO	8086h	**Vendor Identification (VID1):** PCI standard identification for Intel.

6.2 DID1—Device Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 2–3h
Default Value: 29E1h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:8	RO	29h	**Device Identification Number (DID1(UB)):** Identifier assigned to the MCH device 1 (virtual PCI-to-PCI bridge, PCI Express port).
7:4	RO	Eh	**Device Identification Number (DID1(HW)):** Identifier assigned to the MCH device 1 (virtual PCI-to-PCI bridge, PCI Express port).
3:0	RO	1h	**Device Identification Number (DID1(LB)):** Identifier assigned to the MCH device 1 (virtual PCI-to-PCI bridge, PCI Express port).

6.3 PCICMD1—PCI Command

B/D/F/Type: 0/1/0/PCI
Address Offset: 4–5h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	00h	Reserved
10	RW	0b	**INTA Assertion Disable (INTAAD):** 0 = This device is permitted to generate INTA interrupt messages. 1 = This device is prevented from generating interrupt messages. Any INTA emulation interrupts already asserted must be de-asserted when this bit is set. Only affects interrupts generated by the device (PCI INTA from a PME event) controlled by this command register. It does not affect upstream MSIs, upstream PCI INTA-INTD assert and de-assert messages.
9	RO	0b	**Fast Back-to-Back Enable (FB2B):** Not Applicable or Implemented. Hardwired to 0.

Bit	Access	Default Value	Description
8	RW	0b	**SERR# Message Enable (SERRE1):** Controls Device 1 SERR# messaging. The MCH communicates the SERR# condition by sending an SERR message to the ICH. This bit, when set, enables reporting of non-fatal and fatal errors detected by the device to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI-Express specific bits in the Device Control Register. 0 = The SERR message is generated by the MCH for Device 1 only under conditions enabled individually through the Device Control Register. 1 = The MCH is enabled to generate SERR messages which will be sent to the ICH for specific Device 1 error conditions generated/detected on the primary side of the virtual PCI to PCI bridge (not those received by the secondary side). The status of SERRs generated is reported in the PCISTS1 register.
7	RO	0b	Reserved
6	RW	0b	**Parity Error Response Enable (PERRE):** Controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0 = Master Data Parity Error bit in PCI Status register can NOT be set. 1 = Master Data Parity Error bit in PCI Status register CAN be set.
5:3	RO	0b	Reserved
2	RW	0b	**Bus Master Enable (BME):** Controls the ability of the PCI Express port to forward Memory and IO Read/Write Requests in the upstream direction. 0 = This device is prevented from making memory or IO requests to its primary bus. Note that according to PCI Specification, as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, IO writes/reads, peer writes/reads, and MSIs will all be treated as illegal cycles. Writes are forwarded to memory address C0000h with byte enables de-asserted. Reads will be forwarded to memory address C0000h and will return Unsupported Request status (or Master abort) in its completion packet. 1 = This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus will be issued when the data is available. This bit does not affect forwarding of Completions from the primary interface to the secondary interface.
1	RW	0b	**Memory Access Enable (MAE):** 0 = All of device 1's memory space is disabled. 1 = Enable the Memory and Pre-fetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	RW	0b	**I/O Access Enable (IOAE):** 0 = All of device 1's I/O space is disabled. 1 = Enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers.

6.4 PCISTS1—PCI Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 6–7h
Default Value: 0010h
Access: RO, RWC
Size: 16 bits

This register reports the occurrence of error conditions associated with primary side of the "virtual" Host-PCI Express bridge embedded within the MCH.

Bit	Access	Default Value	Description
15	RO	0b	**Detected Parity Error (DPE):** Not Applicable or Implemented. Hardwired to 0. Parity (generating poisoned Transaction Layer Packets) is not supported on the primary side of this device.
14	RWC	0b	**Signaled System Error (SSE):** This bit is set when this Device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is 1. Both received (if enabled by BCTRL1[1]) and internally detected error messages do not affect this field.
13	RO	0b	**Received Master Abort Status (RMAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a master abort does not exist on primary side of this device.
12	RO	0b	**Received Target Abort Status (RTAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
11	RO	0b	**Signaled Target Abort Status (STAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	RO	00b	**DEVSELB Timing (DEVT):** This device is not the subtractively decoded device on bus 0. This bit field is therefore hardwired to 00 to indicate that the device uses the fastest possible decode.
8	RO	0b	**Master Data Parity Error (PMDPE):** Because the primary side of the PCI Express's virtual peer-to-peer bridge is integrated with the MCH functionality, there is no scenario where this bit will get set. Because hardware will never set this bit, it is impossible for software to have an opportunity to clear this bit or otherwise test that it is implemented. The PCI specification defines it as a R/WC, but for our implementation an RO definition behaves the same way and will meet all Microsoft testing requirements. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO	0b	**Fast Back-to-Back (FB2B):** Not Applicable or Implemented. Hardwired to 0.
6	RO	0b	Reserved
5	RO	0b	**66/60MHz capability (CAP66):** Not Applicable or Implemented. Hardwired to 0.
4	RO	1b	**Capabilities List (CAPL):** Indicates that a capabilities list is present. Hardwired to 1.
3	RO	0b	**INTA Status (INTAS):** Indicates that an interrupt message is pending internally to the device. Only PME sources feed into this status bit (not PCI INTA-INTD assert and de-assert messages). The INTA Assertion Disable bit, PCICMD1[10], has no effect on this bit.
2:0	RO	000b	Reserved

6.5 RID1—Revision Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 8h
Default Value: see table below
Access: RO
Size: 8 bits

This register contains the revision number of the MCH device 1. These bits are read only and writes to this register have no effect.

Bit	Access	Default Value	Description
7:0	RO	see description	**Revision Identification Number (RID1):** This is an 8-bit value that indicates the revision identification number for the MCH Device 0. Refer to the *Intel® X48 Express Chipset Specification Update* for the value of this register.

6.6 CC1—Class Code

B/D/F/Type: 0/1/0/PCI
Address Offset: 9–Bh
Default Value: 060400h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access	Default Value	Description
23:16	RO	06h	**Base Class Code (BCC):** Indicates the base class code for this device. This code has the value 06h, indicating a Bridge device.
15:8	RO	04h	**Sub-Class Code (SUBCC):** Indicates the sub-class code for this device. The code is 04h indicating a PCI to PCI Bridge.
7:0	RO	00h	**Programming Interface (PI):** Indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

6.7 CL1—Cache Line Size

B/D/F/Type: 0/1/0/PCI
Address Offset: Ch
Default Value: 00h
Access: RW
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RW	00h	**Cache Line Size (Scratch pad):** Implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

6.8 HDR1—Header Type

B/D/F/Type: 0/1/0/PCI
Address Offset: Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access	Default Value	Description
7:0	RO	01h	**Header Type Register (HDR):** Returns 01h to indicate that this is a single function device with bridge header layout.

6.9 PBUSN1—Primary Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that this "virtual" Host-PCI Express bridge is connected to PCI bus 0.

Bit	Access	Default Value	Description
7:0	RO	00h	**Primary Bus Number (BUSN):** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since device 1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0.

6.10 SBUSN1—Secondary Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 19h
Default Value: 00h
Access: RW
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the "virtual" bridge. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express.

Bit	Access	Default Value	Description
7:0	RW	00h	**Secondary Bus Number (BUSN):** This field is programmed by configuration software with the bus number assigned to PCI Express.

6.11 SUBUSN1—Subordinate Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 1Ah
Default Value: 00h
Access: RW
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express.

Bit	Access	Default Value	Description
7:0	RW	00h	**Subordinate Bus Number (BUSN):** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the device 1 bridge. When only a single PCI device resides on the PCI Express segment, this register will contain the same value as the SBUSN1 register.

6.12 IOBASE1—I/O Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 1Ch
Default Value: F0h
Access: RO, RW
Size: 8 bits

This register controls the processor to PCI Express I/O access routing based on the following formula:

$$IO\_BASE \leq address \leq IO\_LIMIT$$

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4 KB boundary.

Bit	Access	Default Value	Description
7:4	RW	Fh	**I/O Address Base (IOBASE):** Corresponds to A[15:12] of the I/O addresses passed by bridge 1 to PCI Express.
3:0	RO	0h	Reserved

6.13 IOLIMIT1—I/O Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 1Dh
Default Value: 00h
Access: RW, RO
Size: 8 bits

This register controls the processor to PCI Express I/O access routing based on the following formula:

$$IO\_BASE \leq address \leq IO\_LIMIT$$

Only upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4 KB aligned address block.

Bit	Access	Default Value	Description
7:4	RW	0h	**I/O Address Limit (IOLIMIT):** Corresponds to A[15:12] of the I/O address limit of device #1. Devices between this upper limit and IOBASE1 will be passed to the PCI Express hierarchy associated with this device.
3:0	RO	0h	Reserved

6.14 SSTS1—Secondary Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 1E–1Fh
Default Value: 0000h
Access: RO, RWC
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side of the "virtual" PCI-PCI bridge embedded within MCH.

Bit	Access	Default Value	Description
15	RWC	0b	**Detected Parity Error (DPE):** This bit is set by the Secondary Side for a Type 1 Configuration Space header device whenever it receives a Poisoned Transaction Layer Packet, regardless of the state of the Parity Error Response Enable bit in the Bridge Control Register.
14	RWC	0b	**Received System Error (RSE):** This bit is set when the Secondary Side for a Type 1 configuration space header device receives an ERR_FATAL or ERR_NONFATAL.
13	RWC	0b	**Received Master Abort (RMA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Unsupported Request Completion Status.
12	RWC	0b	**Received Target Abort (RTA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Completer Abort Completion Status.
11	RO	0b	**Signaled Target Abort (STA):** Not Applicable or Implemented. Hardwired to 0. The MCH does not generate Target Aborts (the MCH will never complete a request using the Completer Abort Completion status).
10:9	RO	00b	**DEVSELB Timing (DEVT):** Not Applicable or Implemented. Hardwired to 0.
8	RWC	0b	**Master Data Parity Error (SMDPE):** When set indicates that the MCH received across the link (upstream) a Read Data Completion Poisoned Transaction Layer Packet (EP=1). This bit can only be set when the Parity Error Enable bit in the Bridge Control register is set.
7	RO	0b	**Fast Back-to-Back (FB2B):** Not Applicable or Implemented. Hardwired to 0.
6	RO	0b	Reserved
5	RO	0b	**66/60 MHz capability (CAP66):** Not Applicable or Implemented. Hardwired to 0.
4:0	RO	00h	Reserved

6.15 MBASE1—Memory Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 20–21h
Default Value: FFF0h
Access: RW, RO
Size: 16 bits

This register controls the processor to PCI Express non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary.

Bit	Access	Default Value	Description
15:4	RW	FFFh	**Memory Address Base (MBASE):** This field corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express.
3:0	RO	0h	Reserved

6.16 MLIMIT1—Memory Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 22–23h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

This register controls the processor to PCI Express non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1 MB aligned memory block.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI Express address ranges (typically where control/status memory-mapped I/O data structures of the controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically device local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved processor- PCI Express memory access performance.

Note: Configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges (i.e., prevent overlap with each other and/or with the ranges covered with the main memory). There is no provision in the MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not ensured.

Bit	Access	Default Value	Description
15:4	RW	000h	**Memory Address Limit (MLIMIT):** This field corresponds to A[31:20] of the upper limit of the address range passed to PCI Express.
3:0	RO	0h	Reserved

6.17 PMBASE1—Prefetchable Memory Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 24–25h
Default Value: FFF1h
Access: RW, RO
Size: 16 bits

This register in conjunction with the corresponding Upper Base Address register controls the processor to PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1MB boundary.

Bit	Access	Default Value	Description
15:4	RW	FFFh	**Prefetchable Memory Base Address (MBASE):** Corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express.
3:0	RO	1h	**64-bit Address Support:** Indicates that the upper 32 bits of the prefetchable memory region base address are contained in the Prefetchable Memory base Upper Address register at 28h.

6.18 PMLIMIT1—Prefetchable Memory Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 26–27h
Default Value: 0001h
Access: RO, RW
Size: 16 bits

This register in conjunction with the corresponding Upper Limit Address register controls the processor to PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1 MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the processor perspective.

Bit	Access	Default Value	Description
15:4	RW	000h	**Prefetchable Memory Address Limit (PMLIMIT):** This field corresponds to A[31:20] of the upper limit of the address range passed to PCI Express.
3:0	RO	1h	**64-bit Address Support:** This field indicates that the upper 32 bits of the prefetchable memory region limit address are contained in the Prefetchable Memory Base Limit Address register at 2Ch

6.19 PMBASEU1—Prefetchable Memory Base Address Upper

B/D/F/Type: 0/1/0/PCI
Address Offset: 28–2Bh
Default Value: 00000000h
Access: RW
Size: 32 bits

The functionality associated with this register is present in the PCI Express design implementation.

This register in conjunction with the corresponding Upper Base Address register controls the processor to PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1MB boundary.

Bit	Access	Default Value	Description
31:0	RW	00000000h	**Prefetchable Memory Base Address (MBASEU):** This field corresponds to A[63:32] of the lower limit of the prefetchable memory range that will be passed to PCI Express.

6.20 PMLIMITU1—Prefetchable Memory Limit Address Upper

B/D/F/Type: 0/1/0/PCI
Address Offset: 2C–2Fh
Default Value: 00000000h
Access: RW
Size: 32 bits

The functionality associated with this register is present in the PCI Express design implementation.

This register in conjunction with the corresponding Upper Limit Address register controls the processor to PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40- bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block.

Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e. prefetchable) from the processor perspective.

Bit	Access	Default Value	Description
31:0	RW	00000000h	**Prefetchable Memory Address Limit (MLIMITU):** This field corresponds to A[63:32] of the upper limit of the prefetchable Memory range that will be passed to PCI Express.

6.21 CAPPTR1—Capabilities Pointer

B/D/F/Type: 0/1/0/PCI
Address Offset: 34h
Default Value: 88h
Access: RO
Size: 8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

Bit	Access	Default Value	Description
7:0	RO	88h	**First Capability (CAPPTR1):** The first capability in the list is the Subsystem ID and Subsystem Vendor ID Capability.

6.22 INTRLINE1—Interrupt Line

B/D/F/Type: 0/1/0/PCI
Address Offset: 3Ch
Default Value: 00h
Access: RW
Size: 8 bits

This register contains interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Bit	Access	Default Value	Description
7:0	RW	00h	**Interrupt Connection (INTCON):** This field is used to communicate interrupt line routing information.

6.23 INTRPIN1—Interrupt Pin

B/D/F/Type: 0/1/0/PCI
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

This register specifies which interrupt pin this device uses.

Bit	Access	Default Value	Description
7:0	RO	01h	**Interrupt Pin (INTPIN):** As a single function device, the PCI Express device specifies INTA as its interrupt pin. 01h=INTA.

6.24 BCTRL1—Bridge Control

B/D/F/Type: 0/1/0/PCI
Address Offset: 3E–3Fh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-PCI bridges. The BCTRL provides additional control for the secondary interface as well as some bits that affect the overall behavior of the "virtual" Host-PCI Express bridge embedded within MCH.

Bit	Access	Default Value	Description
15:12	RO	0h	Reserved
11	RO	0b	**Discard Timer SERR# Enable (DTSERRE):** Not Applicable or Implemented. Hardwired to 0.
10	RO	0b	**Discard Timer Status (DTSTS):** Not Applicable or Implemented. Hardwired to 0.

Bit	Access	Default Value	Description
9	RO	0b	**Secondary Discard Timer (SDT):** Not Applicable or Implemented. Hardwired to 0.
8	RO	0b	**Primary Discard Timer (PDT):** Not Applicable or Implemented. Hardwired to 0.
7	RO	0b	**Fast Back-to-Back Enable (FB2BEN):** Not Applicable or Implemented. Hardwired to 0.
6	RW	0b	**Secondary Bus Reset (SRESET):** Setting this bit triggers a hot reset on the corresponding PCI Express Port. This will force the LTSSM to transition to the Hot Reset state (via Recovery) from L0 or L1 states.
5	RO	0b	**Master Abort Mode (MAMODE):** Does not apply to PCI Express. Hardwired to 0.
4	RW	0b	**VGA 16-bit Decode (VGA16D):** Enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if bit 3 (VGA Enable) of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. 0 = Execute 10-bit address decodes on VGA I/O accesses. 1 = Execute 16-bit address decodes on VGA I/O accesses.
3	RW	0b	**VGA Enable (VGAEN):** Controls the routing of processor initiated transactions targeting VGA compatible I/O and memory address ranges. See the VGAEN/MDAP table in device 0, offset 97h[0].
2	RW	0b	**ISA Enable (ISAEN):** Needed to exclude legacy resource decode to route ISA resources to legacy decode path. Modifies the response by the MCH to an I/O access issued by the processor that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions will be mapped to PCI Express. 1 = MCH will not forward to PCI Express any I/O transactions addressing the last 768 bytes in each 1KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers.
1	RW	0b	**SERR Enable (SERREN):** 0 = No forwarding of error messages from secondary side to primary side that could result in an SERR. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.
0	RW	0b	**Parity Error Response Enable (PEREN):** Controls whether or not the Master Data Parity Error bit in the Secondary Status register is set when the MCH receives across the link (upstream) a Read Data Completion Poisoned Transaction Layer Packet. 0 = Master Data Parity Error bit in Secondary Status register can NOT be set. 1 = Master Data Parity Error bit in Secondary Status register CAN be set.

6.25 PM_CAPID1—Power Management Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: 80–83h
Default Value: C8039001h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:27	RO	19h	**PME Support (PMES):** This field indicates the power states in which this device may indicate PME wake via PCI Express messaging. D0, D3hot & D3cold. This device is not required to do anything to support D3hot & D3cold, it simply must report that those states are supported. Refer to the PCI Power Management 1.1 specification for encoding explanation and other power management details.
26	RO	0b	**D2 Power State Support (D2PSS):** Hardwired to 0 to indicate that the D2 power management state is NOT supported.
25	RO	0b	**D1 Power State Support (D1PSS):** Hardwired to 0 to indicate that the D1 power management state is NOT supported.
24:22	RO	000b	**Auxiliary Current (AUXC):** Hardwired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.
21	RO	0b	**Device Specific Initialization (DSI):** Hardwired to 0 to indicate that special initialization of this device is NOT required before generic class device driver is to use it.
20	RO	0b	**Auxiliary Power Source (APS):** Hardwired to 0.
19	RO	0b	**PME Clock (PMECLK):** Hardwired to 0 to indicate this device does NOT support PMEB generation.
18:16	RO	011b	**PCI PM CAP Version (PCIPMCV):** A value of 011b indicates that this function complies with revision 1.2 of the PCI Power Management Interface Specification.
15:8	RO	90h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, then the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h.
7:0	RO	01h	**Capability ID (CID):** Value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.

6.26 PM_CS1—Power Management Control/Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 84–87h
Default Value: 00000008h
Access: RO, RW, RW/P
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	Reserved
15	RO	0b	**PME Status (PMESTS):** Indicates that this device does not support PMEB generation from D3cold.
14:13	RO	00b	**Data Scale (DSCALE):** Indicates that this device does not support the power management data register.
12:9	RO	0h	**Data Select (DSEL):** Indicates that this device does not support the power management data register.
8	RW/P	0b	**PME Enable (PMEE):** Indicates that this device does not generate PMEB assertion from any D-state. 0 = PMEB generation not possible from any D State 1 = PMEB generation enabled from any D State The setting of this bit has no effect on hardware. See PM_CAP[15:11]
7:2	RO	0000b	Reserved
1:0	RW	00b	**Power State (PS):** Indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00 = D0 11 = D3 Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state in order to be fully-functional. When the Power State is other than D0, the bridge will Master Abort (i.e. not claim) any downstream cycles (with exception of type 0 configuration cycles). Consequently, these unclaimed cycles will go down DMI and come back up as Unsupported Requests, which the MCH logs as Master Aborts in Device 0 PCISTS[13] There is no additional hardware functionality required to support these Power States.

6.27 SS_CAPID—Subsystem ID and Vendor ID Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: 88–8Bh
Default Value: 0000800Dh
Access: RO
Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides. Because this device is an integrated part of the system and not an add-in device, it is anticipated that this capability will never be used. However, it is necessary because Microsoft will test for its presence.

Bit	Access	Default Value	Description
31:16	RO	0000h	Reserved
15:8	RO	80h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list which is the PCI Power Management capability.
7:0	RO	0Dh	**Capability ID (CID):** Value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI Bridge.

6.28 SS—Subsystem ID and Subsystem Vendor ID

B/D/F/Type: 0/1/0/PCI
Address Offset: 8C–8Fh
Default Value: 00008086h
Access: RWO
Size: 32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and a hardware reset.

Bit	Access	Default Value	Description
31:16	RWO	0000h	**Subsystem ID (SSID):** Identifies the particular subsystem and is assigned by the vendor.
15:0	RWO	8086h	**Subsystem Vendor ID (SSVID):** Identifies the manufacturer of the subsystem and is the same as the vendor ID which is assigned by the PCI Special Interest Group.

6.29 MSI_CAPID—Message Signaled Interrupts Capability ID

B/D/F/Type: 0/1/0/PCI
Address Offset: 90–91h
Default Value: A005h
Access: RO
Size: 16 bits

When a device supports MSI, it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

Bit	Access	Default Value	Description
15:8	RO	A0h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list which is the PCI Express capability.
7:0	RO	05h	**Capability ID (CID):** Value of 05h identifies this linked list item (capability structure) as being for MSI registers.

6.30 MC—Message Control

B/D/F/Type: 0/1/0/PCI
Address Offset: 92–93h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so.

If the device writes the same message multiple times, only one of those messages is ensured to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access	Default Value	Description
15:8	RO	00h	Reserved
7	RO	0b	**64-bit Address Capable (64AC):** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address.
6:4	RW	000b	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
3:1	RO	000b	**Multiple Message Capable (MMC):** System software reads this field to determine the number of messages being requested by this device. The value of 000b equates to 1 message requested. 000 = 1 message requested All other encodings are reserved.
0	RW	0b	**MSI Enable (MSIEN):** Controls the ability of this device to generate MSIs. 0 = 0MSI will not be generated. 1 = MSI will be generated when we receive PME messages. INTA will not be generated and INTA Status (PCISTS1[3]) will not be set.

6.31 MA—Message Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 94–97h
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

Bit	Access	Default Value	Description
31:2	RW	00000000h	**Message Address (MA):** Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO	00b	**Force DWord Align (FDWA):** Hardwired to 0 so that addresses assigned by system software are always aligned on a dword address boundary.

6.32 MD—Message Data

B/D/F/Type: 0/1/0/PCI
Address Offset: 98–99h
Default Value: 0000h
Access: RW
Size: 16 bits

Bit	Access	Default Value	Description
15:0	RW	0000h	**Message Data (MD):** Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16-bits are always set to 0. The lower 16-bits are supplied by this register.

6.33 PE_CAPL—PCI Express* Capability List

B/D/F/Type: 0/1/0/PCI
Address Offset: A0–A1h
Default Value: 0010h
Access: RO
Size: 16 bits

This register enumerates the PCI Express capability structure.

Bit	Access	Default Value	Description
15:8	RO	00h	**Pointer to Next Capability (PNC):** This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express Extended Configuration Space.
7:0	RO	10h	**Capability ID (CID):** Identifies this linked list item (capability structure) as being for PCI Express registers.

6.34 PE_CAP—PCI Express* Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: A2–A3h
Default Value: 0142h
Access: RO, RWO
Size: 16 bits

This register indicates PCI Express device capabilities.

Bit	Access	Default Value	Description
15:14	RO	00b	Reserved
13:9	RO	00h	**Interrupt Message Number (IMN):** Not Applicable or Implemented. Hardwired to 0.
8	RWO	1b	**Slot Implemented (SI):** 0 = The PCI Express Link associated with this port is connected to an integrated component or is disabled. 1 = The PCI Express Link associated with this port is connected to a slot.
7:4	RO	4h	**Device/Port Type (DPT):** Hardwired to 4h to indicate root port of PCI Express Root Complex.
3:0	RO	2h	**PCI Express Capability Version (PCIECV):** Hardwired to 2h to indicate compliance to the PCI Express Capabilities Register Expansion ECN.

6.35 DCAP—Device Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: A4–A7h
Default Value: 00008000h
Access: RO
Size: 32 bits

This register indicates PCI Express device capabilities.

Bit	Access	Default Value	Description
31:16	RO	0000h	Reserved
15	RO	1b	**Role Based Error Reporting (RBER):** Role Based Error Reporting (RBER): Indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 1.1 spec.
14:6	RO	000h	Reserved
5	RO	0b	**Extended Tag Field Supported (ETFS):** Hardwired to indicate support for 5-bit Tags as a Requestor.
4:3	RO	00b	**Phantom Functions Supported (PFS):** Not Applicable or Implemented. Hardwired to 0.
2:0	RO	000b	**Max Payload Size (MPS):** Hardwired to indicate 128B max supported payload for Transaction Layer Packets (TLP).

6.36 DCTL—Device Control

B/D/F/Type: 0/1/0/PCI
Address Offset: A8–A9h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

This register provides control for PCI Express device specific capabilities.

The error reporting enable bits are in reference to errors detected by this device, not error messages received across the link. The reporting of error messages (ERR_CORR, ERR_NONFATAL, ERR_FATAL) received by Root Port is controlled exclusively by Root Port Command Register.

Bit	Access	Default Value	Description
15:8	RO	0h	Reserved
7:5	RW	000b	**Max Payload Size (MPS):** 000 = 128B max supported payload for Transaction Layer Packets (TLP). As a receiver, the Device must handle TLPs as large as the set value; as transmitter, the Device must not generate TLPs exceeding the set value. All other encodings are reserved. Hardware will actually ignore this field. It is writeable only to support compliance testing.
4	RO	0b	Reserved.
3	RW	0b	**Unsupported Request Reporting Enable (URRE):** When set, this bit allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_CORR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_CORR is signaled when an unmasked Advisory Non-Fatal UR is received. An ERR_FATAL or ERR_NONFATAL is sent to the Root Control register when an uncorrectable non-Advisory UR is received with the severity bit set in the Uncorrectable Error Severity register.
2	RW	0b	**Fatal Error Reporting Enable (FERE):** When set, this bit enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	RW	0b	**Non-Fatal Error Reporting Enable (NERE):** When set, this bit enables signaling of ERR_NONFATAL to the Rool Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	RW	0b	**Correctable Error Reporting Enable (CERE):** When set, this bit enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

6.37 DSTS—Device Status

B/D/F/Type: 0/1/0/PCI
Address Offset: AA–ABh
Default Value: 0000h
Access: RO, RWC
Size: 16 bits

Reflects status corresponding to controls in the Device Control register. The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

Bit	Access	Default Value	Description
15:6	RO	000h	Reserved
5	RO	0b	**Transactions Pending (TP):** 0 = All pending transactions (including completions for any outstanding non-posted requests on any used virtual channel) have been completed. 1 = Indicates that the device has transaction(s) pending (including completions for any outstanding non-posted requests for all used Traffic Classes).
4	RO	0b	Reserved
3	RWC	0b	**Unsupported Request Detected (URD):** When set, this bit indicates that the Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register. Additionally, the Non-Fatal Error Detected bit or the Fatal Error Detected bit is set according to the setting of the Unsupported Request Error Severity bit. In production systems setting the Fatal Error Detected bit is not an option as support for AER will not be reported.
2	RWC	0b	**Fatal Error Detected (FED):** When set, this bit indicates that fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
1	RWC	0b	**Non-Fatal Error Detected (NFED):** When set, this bit indicates that non-fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
0	RWC	0b	**Correctable Error Detected (CED):** When set, this bit indicates that correctable error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the correctable error mask register.

6.38 LCAP—Link Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: AC–AFh
Default Value: 02214D02h
Access: RO, RWO
Size: 32 bits

This register indicates PCI Express device specific capabilities.

Bit	Access	Default Value	Description
31:24	RO	02h	**Port Number (PN):** This field indicates the PCI Express port number for the given PCI Express link. Matches the value in Element Self Description[31:24].
23:22	RO	000b	Reserved
21	RO	1b	**Link Bandwidth Notification Capability:** A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. This capability is required for all Root Ports and Switch downstream ports supporting Links wider than x1 and/or multiple Link speeds. This field is not applicable and is reserved for Endpoint devices, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Devices that do not implement the Link Bandwidth Notification capability must hardwire this bit to 0b.
20	RO	0b	**Data Link Layer Link Active Reporting Capable (DLLLARC):** For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.
19	RO	0b	**Surprise Down Error Reporting Capable (SDERC):** For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.
18	RO	0b	**Clock Power Management (CPM):** A value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) when the link is in the L1 and L2/3 Ready link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these link states. This capability is applicable only in form factors that support "clock request" (CLKREQ#) capability. For a multi-function device, each function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the multifunction device indicate a 1b in this bit.
17:15	RWO	010b	**L1 Exit Latency (L1ELAT):** Indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010 b indicates the range of 2 us to less than 4 us. Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.
14:12	RO	100b	Reserved
11:10	RWO	11b	**Active State Link PM Support (ASLPMS):** The MCH supports ASPM L1.

Bit	Access	Default Value	Description
9:4	RO	10h	**Max Link Width (MLW):** This field indicates the maximum number of lanes supported for this link. 10h = x16
3:0	RWO	2h	**Max Link Speed (MLS):** Supported Link Speed - This field indicates the supported Link speed(s) of the associated Port. 0001b = 2.5 GT/s Link speed supported 0010b = 5.0 GT/s and 2.5 GT/s Link speeds supported All other encodings are reserved.

6.39 LCTL—Link Control

B/D/F/Type: 0/1/0/PCI
Address Offset: B0–B1h
Default Value: 0000h
Access: RO, RW, RW/SC
Size: 16 bits

This register allows control of PCI Express link.

Bit	Access	Default Value	Description
15:12	RO	0000b	Reserved
11	RW	0b	**Link Autonomous Bandwidth Interrupt Enable:** When set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set. This bit is not applicable and is reserved for Endpoint devices, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Devices that do not implement the Link Bandwidth Notification capability must hardwire this bit to 0b.
10	RW	0b	**Link Bandwidth Management Interrupt Enable:** When set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set. This bit is not applicable and is reserved for Endpoint devices, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches.
9	RO	0b	**Hardware Autonomous Width Disable:** When set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Devices that do not implement the ability autonomously to change Link width are permitted to hardwire this bit to 0b. The MCH does not support autonomous width change. So, this bit is "RO".
8	RO	0b	**Enable Clock Power Management (ECPM):** Applicable only for form factors that support a "Clock Request" (CLKREQ#) mechanism, this enable functions as follows: 0 = Clock power management is disabled and device must hold CLKREQ# signal low 1 = When this bit is set to 1 the device is permitted to use CLKREQ# signal to power manage link clock according to protocol defined in appropriate form factor specification. Default value of this field is 0b. Components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities Register) must hardwire this bit to 0b.
7	RW	0b	**Extended Synch (ES):** 0 = Standard Fast Training Sequence (FTS). 1 = Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state. This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and symbol lock before the link enters L0 and resumes communication. This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns. **NOTE:** The 82X48 MCH does not support L0s.

Bit	Access	Default Value	Description
6	RW	0b	**Common Clock Configuration (CCC):** 0 = Indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. 1 = Indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock.
5	RW/SC	0b	**Retrain Link (RL):** 0 = Normal operation. 1 = Full Link retraining is initiated by directing the Physical Layer LTSSM from L0 or L1 states to the Recovery state. This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0). It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	RW	0b	**Link Disable (LD):** 0 = Normal operation. 1 = Link is disabled. Forces the LTSSM to transition to the Disabled state (via Recovery) from L0 or L1 states. Link retraining happens automatically on 0-to-1 transition, just like when coming out of reset. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.
3	RO	0b	**Read Completion Boundary (RCB):** Hardwired to 0 to indicate 64 byte.
2	RO	0b	Reserved
1:0	RW	00b	**Active State PM (ASPM):** Controls the level of active state power management supported on the given link. 00 = Disabled 01 = Reserved 10 = Reserved 11 = L1 Entry Supported

6.40 LSTS—Link Status

B/D/F/Type: 0/1/0/PCI
Address Offset: B2–B3h
Default Value: 1000h
Access: RWC, RO
Size: 16 bits

This register indicates PCI Express link status.

Bit	Access	Default Value	Description
15	RWC	0b	**Link Autonomous Bandwidth Status (LABWS):** This bit is set to 1b by hardware to indicate that hardware has autonomously changed link speed or width, without the port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the downstream component that was indicated as an autonomous change.
14	RWC	0b	**Link Bandwidth Management Status (LBWMS):** This bit is set to 1b by hardware to indicate that either of the following has occurred without the port transitioning through DL_Down status: A link retraining initiated by a write of 1b to the Retrain Link bit has completed. **NOTE:** This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. Hardware has autonomously changed link speed or width to attempt to correct unreliable link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the downstream component that was not indicated as an autonomous change.
13	RO	0b	**Data Link Layer Link Active (Optional) (DLLLA):** This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. This bit must be implemented if the corresponding Data Link Layer Active Capability bit is implemented. Otherwise, this bit must be hardwired to 0b.
12	RO	1b	**Slot Clock Configuration (SCC):** 0 = The device uses an independent clock irrespective of the presence of a reference on the connector. 1 = The device uses the same physical reference clock that the platform provides on the connector.
11	RO	0b	**Link Training (LTRN):** Indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state once Link training is complete.
10	RO	0b	**Undefined:** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.

Bit	Access	Default Value	Description
9:4	RO	00h	**Negotiated Link Width (NLW):** Indicates negotiated link width. This field is valid only when the link is in the L0 or L1 states (after link width negotiation is successfully completed). 01h = x1 04h = ‘x4 — This is not a supported PCIe Gen2.0 link width. Link width x4 is only valid when PCIe Gen1.1 I/O card is used in the secondary port. 08h = x8 — This is not a supported PCIe Gen2.0 link width. Link width x8 is only valid when PCIe Gen1.1 I/O card is used in the secondary port. 10h = x16 All other encodings are reserved.
3:0	RO	0h	**Current Link Speed (CLS):** This field indicates the negotiated Link speed of the given PCI Express Link. 0001b = 2.5 GT/s PCI Express Link 0010b = 5 GT/s PCI Express Link All other encodings are reserved. The value in this field is undefined when the Link is not up.

6.41 SLOTCAP—Slot Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: B4–B7h
Default Value: 00040000h
Access: RWO, RO
Size: 32 bits

PCI Express Slot related registers.

Bit	Access	Default Value	Description
31:19	RWO	0000h	**Physical Slot Number (PSN):** Indicates the physical slot number attached to this Port.
18	RO	1b	Reserved
17	RO	0b	**Electromechanical Interlock Present (EIP):** When set to 1b, this bit indicates that an Electromechanical Interlock is implemented on the chassis for this slot.
16:15	RWO	00b	**Slot Power Limit Scale (SPLS):** Specifies the scale used for the Slot Power Limit Value. 00 = 1.0x 01 = 0.1x 10 = 0.01x 11 = 0.001x If this field is written, the link sends a Set_Slot_Power_Limit message.
14:7	RWO	00h	**Slot Power Limit Value (SPLV):** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. If this field is written, the link sends a Set_Slot_Power_Limit message.
6:5	RO	00b	Reserved

Bit	Access	Default Value	Description
4	RO	0b	**Power Indicator Present (PIP):** When set to 1b, this bit indicates that a Power Indicator is electrically controlled by the chassis for this slot.
3	RO	0b	**Attention Indicator Present (AIP):** When set to 1b, this bit indicates that an Attention Indicator is electrically controlled by the chassis.
2	RO	0b	**MRL Sensor Present (MSP):** When set to 1b, this bit indicates that an MRL Sensor is implemented on the chassis for this slot.
1	RO	0b	**Power Controller Present (PCP):** When set to 1b, this bit indicates that a software programmable Power Controller is implemented for this slot/adapter (depending on form factor).
0	RO	0b	**Attention Button Present (ABP):** When set to 1b, this bit indicates that an Attention Button for this slot is electrically controlled by the chassis.

6.42 SLOTCTL—Slot Control

B/D/F/Type: 0/1/0/PCI
Address Offset: B8–B9h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

PCI Express Slot related registers.

Bit	Access	Default Value	Description
15:13	RO	000b	Reserved
12	RO	0b	**Data Link Layer State Changed Enable (DLLSCE):** If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed. If the Data Link Layer Link Active capability is not implemented, this bit is permitted to be read-only with a value of 0b.
11	RO	0b	**Electromechanical Interlock Control (EIC):** If an Electromechanical Interlock is implemented, a write of 1b to this field causes the state of the interlock to toggle. A write of 0b to this field has no effect. A read to this register always returns a 0.
10	RO	0b	**Power Controller Control (PCC):** If a Power Controller is implemented, this field when written sets the power state of the slot per the defined encodings. Reads of this field must reflect the value from the latest write, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. Depending on the form factor, the power is turned on/off either to the slot or within the adapter. Note that in some cases the power controller may autonomously remove slot power or not respond to a power-up request based on a detected fault condition, independent of the Power Controller Control setting. The defined encodings are: 0 = Power On 1 = Power Off If the Power Controller Implemented field in the Slot Capabilities register is set to 0b, then writes to this field have no effect and the read value of this field is undefined.

Bit	Access	Default Value	Description
9:8	RO	00b	**Power Indicator Control (PIC):** If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 00 = Reserved 01 = On 10 = Blink 11 = Off If the Power Indicator Present bit in the Slot Capabilities register is 0b, this field is permitted to be read-only with a value of 00b.
7:6	RO	00b	**Attention Indicator Control (AIC):** If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Reads of this field must reflect the value from the latest write, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. If the indicator is electrically controlled by chassis, the indicator is controlled directly by the downstream port through implementation specific mechanisms. 00 = Reserved 01 = On 10 = Blink 11 = Off If the Attention Indicator Present bit in the Slot Capabilities register is 0b, this field is permitted to be read only with a value of 00b.
5:4	RO	00b	Reserved
3	RW	0b	**Presence Detect Changed Enable (PDCE):** When set to 1b, this bit enables software notification on a presence detect changed event.
2	RO	0b	**MRL Sensor Changed Enable (MSCE):** When set to 1b, this bit enables software notification on a MRL sensor changed event. Default value of this field is 0b. If the MRL Sensor Present field in the Slot Capabilities register is set to 0b, this bit is permitted to be read-only with a value of 0b.
1	RO	0b	**Power Fault Detected Enable (PFDE):** When set to 1b, this bit enables software notification on a power fault event. Default value of this field is 0b. If Power Fault detection is not supported, this bit is permitted to be read-only with a value of 0b
0	RO	0b	**Button Pressed Enable (ABPE):** When set to 1b, this bit enables software notification on an attention button pressed event.

6.43 SLOTSTS—Slot Status

B/D/F/Type: 0/1/0/PCI
Address Offset: BA–BBh
Default Value: 0000h
Access: RO, RWC
Size: 16 bits

PCI Express Slot related registers.

Bit	Access	Default Value	Description
15:7	RO	0000000b	Reserved
6	RO	0b	**Presence Detect State (PDS):** This bit indicates the presence of an adapter in the slot, reflected by the logical "OR" of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. 0 = Slot Empty 1 = Card Present in Slot This register must be implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities Register is 0b), this bit must return 1b.
5:4	RO	00b	Reserved
3	RWC	0b	**Detect Changed (PDC):** This bit is set when the value reported in Presence Detect State is changed.
2	RO	0b	**MRL Sensor Changed (MSC):** If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be set.
1	RO	0b	**Power Fault Detected (PFD):** If a Power Controller that supports power fault detection is implemented, this bit is set when the Power Controller detects a power fault at this slot. Note that, depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be set.
0	RO	0b	**Attention Button Pressed (ABP):** If an Attention Button is implemented, this bit is set when the attention button is pressed. If an Attention Button is not supported, this bit must not be set.

6.44 RCTL—Root Control

B/D/F/Type: 0/1/0/PCI
Address Offset: BC–BDh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when our device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR as controlled by these bits takes precedence over the SERR Enable in the PCI Command Register.

Bit	Access	Default Value	Description
15:4	RO	000h	Reserved
3	RW	0b	**PME Interrupt Enable (PMEIE):** 0 = No interrupts are generated as a result of receiving PME messages. 1 = Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status Register. A PME interrupt is also generated if the PME Status bit of the Root Status Register is set when this bit is set from a cleared state.
2	RW	0b	**System Error on Fatal Error Enable (SEFEE):** Controls the Root Complex's response to fatal errors. 0 = No SERR generated on receipt of fatal error. 1 = Indicates that an SERR should be generated if a fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
1	RW	0b	**System Error on Non-Fatal Uncorrectable Error Enable (SENFUEE):** Controls the Root Complex's response to non-fatal errors. 0 = No SERR generated on receipt of non-fatal error. 1 = Indicates that an SERR should be generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
0	RW	0b	**System Error on Correctable Error Enable (SECEE):** Controls the Root Complex's response to correctable errors. 0 = No SERR generated on receipt of correctable error. 1 = Indicates that an SERR should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.

6.45 RSTS—Root Status

B/D/F/Type: 0/1/0/PCI
Address Offset: C0–C3h
Default Value: 00000000h
Access: RO, RWC
Size: 32 bits

This register provides information about PCI Express Root Complex specific parameters.

Bit	Access	Default Value	Description
31:18	RO	0000h	Reserved
17	RO	0b	**PME Pending (PMEP):** Indicates that another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16	RWC	0b	**PME Status (PMES):** Indicates that PME was asserted by the requestor ID indicated in the PME Requestor ID field. Subsequent PMEs are kept pending until the status register is cleared by writing a 1 to this field.
15:0	RO	0000h	**PME Requestor ID (PMERID):** Indicates the PCI requestor ID of the last PME requestor.

6.46 PELC—PCI Express Legacy Control

B/D/F/Type: 0/1/0/PCI
Address Offset: EC–EFh
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

This register controls functionality that is needed by Legacy (non-PCI Express aware) OSs during run time.

Bit	Access	Default Value	Description
31:3	RO	0000000 0h	Reserved
2	RW	0b	**PME GPE Enable (PMEGPE):** 0 = Do not generate GPE PME message when PME is received. 1 = Generate a GPE PME message when PME is received (Assert_PMEGPE and Deassert_PMEGPE messages on DMI). This enables the MCH to support PMEs on the PCI Express port under legacy OSs.
1	RO	0b	Reserved
0	RW	0b	**General Message GPE Enable (GENGPE):** 0 = Do not forward received GPE assert/de-assert messages. 1 = Forward received GPE assert/de-assert messages. These general GPE message can be received via the PCI Express port from an external Intel device and will be subsequently forwarded to the ICH (via Assert_GPE and Deassert_GPE messages on DMI).

6.47 VCECH—Virtual Channel Enhanced Capability Header

B/D/F/Type: 0/1/0/MMR
Address Offset: 100–103h
Default Value: 14010002h
Access: RO
Size: 32 bits

This register indicates PCI Express device Virtual Channel capabilities. Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

Bit	Access	Default Value	Description
31:20	RO	140h	**Pointer to Next Capability (PNC):** The Link Declaration Capability is the next in the PCI Express extended capabilities list.
19:16	RO	1h	**PCI Express Virtual Channel Capability Version (PCIEVCCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. Note: This version does not change for 2.0 compliance.
15:0	RO	0002h	**Extended Capability ID (ECID):** Value of 0002 h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

6.48 PVCCAP1—Port VC Capability Register 1

B/D/F/Type: 0/1/0/MMR
Address Offset: 104–107h
Default Value: 00000000h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:7	RO	00000h	Reserved
6:4	RO	000b	**Low Priority Extended VC Count (LPEVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO	0b	Reserved
2:0	RO	000b	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

6.49 PVCCAP2—Port VC Capability Register 2

B/D/F/Type: 0/1/0/MMR
Address Offset: 108–10Bh
Default Value: 00000000h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:24	RO	00h	**VC Arbitration Table Offset (VCATO):** Indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Capability Structure. A value of 0 indicates that the table is not present (due to fixed VC priority).
23:0	RO	0000h	Reserved

6.50 PVCCTL—Port VC Control

B/D/F/Type: 0/1/0/MMR
Address Offset: 10C–10Dh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

Bit	Access	Default Value	Description
15:4	RO	000h	Reserved
3:1	RW	000b	**VC Arbitration Select (VCAS):** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. Since there is no other VC supported than the default, this field is reserved.
0	RO	0b	Reserved

6.51 VC0RCAP—VC0 Resource Capability

B/D/F/Type: 0/1/0/MMR
Address Offset: 110–113h
Default Value: 00000001h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	Reserved
15	RO	0b	**Reject Snoop Transactions (RSNPT):** 0 = Transactions with or without the No Snoop bit set within the Transaction Layer Packet header are allowed on this VC. 1 = When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
14:8	RO	0000h	Reserved
7:0	RO	01h	**Port Arbitration Capability:** Indicates types of Port Arbitration supported by the VC resource. This field is valid for all Switch Ports, Root Ports that support peer-to-peer traffic, and RCRBs, but not for PCI Express Endpoint devices or Root Ports that do not support peer to peer traffic. Each bit location within this field corresponds to a Port Arbitration Capability defined below. When more than one bit in this field is Set, it indicates that the VC resource can be configured to provide different arbitration services. Software selects among these capabilities by writing to the Port Arbitration Select field (see below). Defined bit positions are: Bit[0] = Default = 01b; Non-configurable hardware-fixed arbitration scheme, e.g., Round Robin (RR) Bit[1] = Weighted Round Robin (WRR) arbitration with 32 phases Bit[2] = WRR arbitration with 64 phases Bit[3] = WRR arbitration with 128 phases Bit[4] = Time-based WRR with 128 phases Bit[5] = WRR arbitration with 256 phases Bits[6:7] = Reserved MCH default indicates "Non-configurable hardware-fixed arbitration scheme".

6.52 VC0RCTL—VC0 Resource Control

B/D/F/Type: 0/1/0/MMR
Address Offset: 114–117h
Default Value: 800000FFh
Access: RO, RW
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access	Default Value	Description
31	RO	1b	**VC0 Enable (VC0E):** For VC0, this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO	0h	Reserved
26:24	RO	000b	**VC0 ID (VC0ID):** Assigns a VC ID to the VC resource. For VC0, this is hardwired to 0 and read only.
23:20	RO	0000h	Reserved
19:17	RW	000b	**Port Arbitration Select:** This field configures the VC resource to provide a particular Port Arbitration service. This field is valid for RCRBs, Root Ports that support peer to peer traffic, and Switch Ports, but not for PCI Express Endpoint devices or Root Ports that do not support peer to peer traffic. The permissible value of this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource.
16:8	RO	00h	Reserved
7:1	RW	7Fh	**TC/VC0 Map (TCVC0M):** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	1b	**TC0/VC0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.

6.53 VC0RSTS—VC0 Resource Status

B/D/F/Type: 0/1/0/MMR
Address Offset: 11A–11Bh
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	Reserved
1	RO	1b	**VC0 Negotiation Pending (VC0NP):** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	Reserved

6.54 RCLDECH—Root Complex Link Declaration Enhanced

B/D/F/Type: 0/1/0/MMR
Address Offset: 140–143h
Default Value: 00010005h
Access: RO
Size: 32 bits

This capability declares links from this element (PCI Express) to other elements of the root complex component to which it belongs. See PCI Express specification for link/ topology declaration requirements.

Bit	Access	Default Value	Description
31:20	RO	000h	**Pointer to Next Capability (PNC):** This is the last capability in the PCI Express extended capabilities list.
19:16	RO	1h	**Link Declaration Capability Version (LDCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. Note: This version does not change for 2.0 compliance.
15:0	RO	0005h	**Extended Capability ID (ECID):** Value of 0005h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

6.55 ESD—Element Self Description

B/D/F/Type: 0/1/0/MMR
Address Offset: 144–147h
Default Value: 02000100h
Access: RO, RWO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access	Default Value	Description
31:24	RO	02h	**Port Number (PN):** Specifies the port number associated with this element with respect to the component that contains this element. This port number value is utilized by the egress port of the component to provide arbitration to this Root Complex Element.
23:16	RWO	00h	**Component ID (CID):** Identifies the physical component that contains this Root Complex Element.
15:8	RO	01h	**Number of Link Entries (NLE):** Indicates the number of link entries following the Element Self Description. This field reports 1 (to Egress port only as we don't report any peer-to-peer capabilities in our topology).
7:4	RO	0h	Reserved
3:0	RO	0h	**Element Type (ET):** Indicates Configuration Space Element.

6.56 LE1D—Link Entry 1 Description

B/D/F/Type: 0/1/0/MMR
Address Offset: 150–153h
Default Value: 00000000h
Access: RO, RWO
Size: 32 bits

This register provides the first part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
31:24	RO	00h	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	RWO	00h	**Target Component ID (TCID):** Identifies the physical or logical component that is targeted by this link entry.
15:2	RO	0000h	Reserved
1	RO	0b	**Link Type (LTYP):** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	RWO	0b	**Link Valid (LV):** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

6.57 LE1A—Link Entry 1 Address

B/D/F/Type: 0/1/0/MMR
Address Offset: 158-15Fh
Default Value: 0000000000000000h
Access: RO, RWO
Size: 64 bits

This register provides the second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:32	RO	00000000h	Reserved
31:12	RWO	00000h	**Link Address (LA):** Memory mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0	RO	000h	Reserved

6.58 PESSTS—PCI Express* Sequence Status

B/D/F/Type: 0/1/0/MMR
Address Offset: 218–21Fh
Default Value: 0000000000000FFFh
Access: RO
Size: 64 bits

PCI Express status reporting that is required by the PCI Express specification.

Bit	Access	Default Value	Description
63:60	RO	0h	Reserved
59:48	RO	000h	**Next Transmit Sequence Number (NTSN):** Value of the NXT_TRANS_SEQ counter. This counter represents the transmit Sequence number to be applied to the next Transaction Layer Packet to be transmitted onto the Link for the first time.
47:44	RO	0h	Reserved
43:32	RO	000h	**Next Packet Sequence Number (NPSN):** Packet sequence number to be applied to the next Transaction Layer Packet to be transmitted or re-transmitted onto the Link.
31:28	RO	0h	Reserved
27:16	RO	000h	**Next Receive Sequence Number (NRSN):** This is the sequence number associated with the Transaction Layer Packet that is expected to be received next.
15:12	RO	0h	Reserved
11:0	RO	FFFh	**Last Acknowledged Sequence Number (LASN):** This is the sequence number associated with the last acknowledged Transaction Layer Packet.

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7 Host-Secondary PCI Express* Bridge Registers (D6:F0)

Device 6 contains the controls associated with the PCI Express root port that is the intended attach point for external devices. In addition, it also functions as the virtual PCI-to-PCI bridge. The table below provides an address map of the D1:F0 registers listed by address offset in ascending order. This chapter provides a detailed bit description of the registers.

Warning: When reading the PCI Express "conceptual" registers such as this, you may not get a valid value unless the register value is stable.

The *PCI Express* Specification* defines two types of reserved bits:

Reserved and Preserved:

- Reserved for future RW implementations; software must preserve value read for writes to bits.
- Reserved and Zero: Reserved for future R/WC/S implementations; software must use 0 for writes to bits.

Unless explicitly documented as Reserved and Zero, all bits marked as reserved are part of the Reserved and Preserved type, which have historically been the typical definition for Reserved.

Note: Most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first disable the link, then program the registers, and then re-enable the link (which will cause a full-retrain with the new settings).

Table 13. Host-Secondary PCI Express* Bridge Register Address Map (D6:F0) (Sheet 1 of 3)

Address Offset	Register Symbol	Register Name	Default Value	Access
0–1h	VID1	Vendor Identification	8086h	RO
2–3h	DID1	Device Identification	29E9h	RO
4–5h	PCICMD1	PCI Command	0000h	RO, RW
6–7h	PCISTS1	PCI Status	0010h	RO, RWC
8h	RID1	Revision Identification	See register description	RO
9–Bh	CC1	Class Code	060400h	RO
Ch	CL1	Cache Line Size	00h	RW
Eh	HDR1	Header Type	01h	RO
18h	PBUSN1	Primary Bus Number	00h	RO
19h	SBUSN1	Secondary Bus Number	00h	RW
1Ah	SUBUSN1	Subordinate Bus Number	00h	RW
1Ch	IOBASE1	I/O Base Address	F0h	RO, RW
1Dh	IOLIMIT1	I/O Limit Address	00h	RW, RO

Table 13. Host-Secondary PCI Express* Bridge Register Address Map (D6:F0) (Sheet 2 of 3)

Address Offset	Register Symbol	Register Name	Default Value	Access
1E–1Fh	SSTS1	Secondary Status	0000h	RO, RWC
20–21h	MBASE1	Memory Base Address	FFF0h	RW, RO
22–23h	MLIMIT1	Memory Limit Address	0000h	RW, RO
24–25h	PMBASE1	Prefetchable Memory Base Address	FFF1h	RW, RO
26–27h	PMLIMIT1	Prefetchable Memory Limit Address	0001h	RO, RW
28–2Bh	PMBASEU1	Prefetchable Memory Base Address Upper	00000000h	RW
2C–2Fh	PMLIMITU1	Prefetchable Memory Limit Address Upper	00000000h	RW
34h	CAPPTR1	Capabilities Pointer	88h	RO
3Ch	INTRLINE1	Interrupt Line	00h	RW
3Dh	INTRPIN1	Interrupt Pin	01h	RO
3E–3Fh	BCTRL1	Bridge Control	0000h	RO, RW
80–83h	PM_CAPID1	Power Management Capabilities	C8039001h	RO
84–87h	PM_CS1	Power Management Control/Status	00000008h	RO, RW, RW/P
88–8Bh	SS_CAPID	Subsystem ID and Vendor ID Capabilities	0000800Dh	RO
8C–8Fh	SS	Subsystem ID and Subsystem Vendor ID	00008086h	RWO
90–91h	MSI_CAPID	Message Signaled Interrupts Capability ID	A005h	RO
92–93h	MC	Message Control	0000h	RW, RO
94–97h	MA	Message Address	00000000h	RO, RW
98–99h	MD	Message Data	0000h	RW
A0–A1h	PE_CAPL	PCI Express Capability List	0010h	RO
A2–A3h	PE_CAP	PCI Express Capabilities	0142h	RO, RWO
A4–A7h	DCAP	Device Capabilities	00008000h	RO
A8–A9h	DCTL	Device Control	0000h	RW, RO
AA–ABh	DSTS	Device Status	0000h	RO, RWC
AC–AFh	LCAP	Link Capabilities	03214D02h	RO, RWO
B0–B1h	LCTL	Link Control	0000h	RO, RW, RW/SC
B2–hB3	LSTS	Link Status	1000h	RWC, RO
B4–B7h	SLOTCAP	Slot Capabilities	00040000h	RWO, RO
B8–B9h	SLOTCTL	Slot Control	0000h	RO, RW
BA–BBh	SLOTSTS	Slot Status	0000h	RO, RWC
BC–BDh	RCTL	Root Control	0000h	RO, RW
C0–C3h	RSTS	Root Status	00000000h	RO, RWC
EC–EFh	PELC	PCI Express Legacy Control	00000000h	RO, RW
100–103h	VCECH	Virtual Channel Enhanced Capability Header	14010002h	RO

Table 13. Host-Secondary PCI Express* Bridge Register Address Map (D6:F0) (Sheet 3 of 3)

Address Offset	Register Symbol	Register Name	Default Value	Access
104–107h	PVCCAP1	Port VC Capability Register 1	00000000h	RO
108–10Bh	PVCCAP2	Port VC Capability Register 2	00000000h	RO
10C–10Dh	PVCCTL	Port VC Control	0000h	RO, RW
110–113h	VC0RCAP	VC0 Resource Capability	00000000h	RO
114–117h	VC0RCTL	VC0 Resource Control	800000FFh	RO, RW
11A–11Bh	VC0RSTS	VC0 Resource Status	0002h	RO
140–143h	RCLDECH	Root Complex Link Declaration Enhanced	00010005h	RO
144–147h	ESD	Element Self Description	03000100h	RO, RWO
150–153h	LE1D	Link Entry 1 Description	00000000h	RO, RWO
158–15Fh	LE1A	Link Entry 1 Address	0000000000 000000h	RO, RWO

7.1 VID1—Vendor Identification

B/D/F/Type: 0/6/0/PCI
Address Offset: 0–1h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identify any PCI device.

Bit	Access	Default Value	Description
15:0	RO	8086h	**Vendor Identification (VID1):** PCI standard identification for Intel.

7.2 DID1—Device Identification

B/D/F/Type: 0/6/0/PCI
Address Offset: 2–3h
Default Value: 29E9h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access	Default Value	Description
15:8	RO	29h	**Device Identification Number (DID1(UB)):** Identifier assigned to the MCH device #6 (virtual PCI-to-PCI bridge, PCI Express port).
7:4	RO	Eh	**Device Identification Number (DID1(HW)):** Identifier assigned to the MCH device #6 (virtual PCI-to-PCI bridge, PCI Express port).
3:0	RO	9h	**Device Identification Number (DID1(LB)):** Identifier assigned to the MCH device #6 (virtual PCI-to-PCI bridge, PCI Express port).

7.3 PCICMD1—PCI Command

B/D/F/Type: 0/6/0/PCI
Address Offset: 4–5h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

Bit	Access	Default Value	Description
15:11	RO	00h	Reserved
10	RW	0b	**INTA Assertion Disable (INTAAD):** 0 = This device is permitted to generate INTA interrupt messages. 1 = This device is prevented from generating interrupt messages. Any INTA emulation interrupts already asserted must be de-asserted when this bit is set. This bit only affects interrupts generated by the device (PCI INTA from a PME event) controlled by this command register. It does not affect upstream MSIs, upstream PCI INTA-INTD assert and de-assert messages.
9	RO	0b	**Fast Back-to-Back Enable (FB2B):** Not Applicable or Implemented. Hardwired to 0.

Bit	Access	Default Value	Description
8	RW	0b	**SERR# Message Enable (SERRE1):** This bit controls Device 6 SERR# messaging. The MCH communicates the SERR# condition by sending a SERR message to the ICH. This bit, when set, enables reporting of non-fatal and fatal errors detected by the device to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI-Express specific bits in the Device Control Register. 0 = The SERR message is generated by the MCH for Device 6 only under conditions enabled individually through the Device Control Register. 1 = The MCH is enabled to generate SERR messages which will be sent to the ICH for specific Device 6 error conditions generated/detected on the primary side of the virtual PCI to PCI bridge (not those received by the secondary side). The status of SERRs generated is reported in the PCISTS1 register.
7	RO	0b	Reserved
6	RW	0b	**Parity Error Response Enable (PERRE):** Controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0 = Master Data Parity Error bit in PCI Status register can NOT be set. 1 = Master Data Parity Error bit in PCI Status register CAN be set.
5:3	RO	0b	Reserved
2	RW	0b	**Bus Master Enable (BME):** Controls the ability of the PCI Express port to forward Memory and I/O Read/Write Requests in the upstream direction. 0 = This device is prevented from making memory or IO requests to its primary bus. Note that according to PCI Specification, as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, IO writes/reads, peer writes/reads, and MSIs will all be treated as illegal cycles. Writes are forwarded to memory address C0000h with byte enables de-asserted. Reads will be forwarded to memory address C0000h and will return Unsupported Request status (or Master abort) in its completion packet. 1 = This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus will be issued when the data is available. This bit does not affect forwarding of Completions from the primary interface to the secondary interface.
1	RW	0b	**Memory Access Enable (MAE):** 0 = All of device #6's memory space is disabled. 1 = Enable the Memory and Pre-fetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	RW	0b	**IO Access Enable (IOAE):** 0 = All of device #6's I/O space is disabled. 1 = Enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers.

7.4 PCISTS1—PCI Status

B/D/F/Type: 0/6/0/PCI
Address Offset: 6–7h
Default Value: 0010h
Access: RO, RWC
Size: 16 bits

This register reports the occurrence of error conditions associated with primary side of the "virtual" Host-PCI Express bridge embedded within the MCH.

Bit	Access	Default Value	Description
15	RO	0b	**Detected Parity Error (DPE):** Not Applicable or Implemented. Hardwired to 0. Parity (generating poisoned Transaction Layer Packets) is not supported on the primary side of this device.
14	RWC	0b	**Signaled System Error (SSE):** This bit is set when this Device sends a SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is 1. Both received (if enabled by BCTRL1[1]) and internally detected error messages do not affect this field).
13	RO	0b	**Received Master Abort Status (RMAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a master abort does not exist on primary side of this device.
12	RO	0b	**Received Target Abort Status (RTAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
11	RO	0b	**Signaled Target Abort Status (STAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	RO	00b	**DEVSELB Timing (DEVT):** This device is not the subtractively decoded device on bus 0. This bit field is therefore hardwired to 00 to indicate that the device uses the fastest possible decode.
8	RO	0b	**Master Data Parity Error (PMDPE):** Because the primary side of the PCI Express's virtual peer-to-peer bridge is integrated with the MCH functionality, there is no scenario where this bit will get set. Because hardware will never set this bit, it is impossible for software to have an opportunity to clear this bit or otherwise test that it is implemented. The PCI specification defines it as a R/WC, but for our implementation an RO definition behaves the same way and will meet all Microsoft testing requirements. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO	0b	**Fast Back-to-Back (FB2B):** Not Applicable or Implemented. Hardwired to 0.
6	RO	0b	Reserved
5	RO	0b	**66/60MHz capability (CAP66):** Not Applicable or Implemented. Hardwired to 0.
4	RO	1b	**Capabilities List (CAPL):** Indicates that a capabilities list is present. Hardwired to 1.
3	RO	0b	**INTA Status (INTAS):** Indicates that an interrupt message is pending internally to the device. Only PME sources feed into this status bit (not PCI INTA-INTD assert and de-assert messages). The INTA Assertion Disable bit, PCICMD1[10], has no effect on this bit.
2:0	RO	000b	Reserved

7.5 RID1—Revision Identification

B/D/F/Type: 0/6/0/PCI
Address Offset: 8h
Default Value: see table below
Access: RO
Size: 8 bits

This register contains the revision number of the MCH device 6. These bits are read only and writes to this register have no effect.

Bit	Access	Default Value	Description
7:0	RO	see description	**Revision Identification Number (RID1):** This is an 8-bit value that indicates the revision identification number for the MCH Device 0. Refer to the *Intel® X48 Express Chipset Specification Update* for the value of this register.

7.6 CC1—Class Code

B/D/F/Type: 0/6/0/PCI
Address Offset: 9–Bh
Default Value: 060400h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access	Default Value	Description
23:16	RO	06h	**Base Class Code (BCC):** Indicates the base class code for this device. This code has the value 06h, indicating a Bridge device.
15:8	RO	04h	**Sub-Class Code (SUBCC):** Indicates the sub-class code for this device. The code is 04h indicating a PCI to PCI Bridge.
7:0	RO	00h	**Programming Interface (PI):** Indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

7.7 CL1—Cache Line Size

B/D/F/Type: 0/6/0/PCI
Address Offset: Ch
Default Value: 00h
Access: RW
Size: 8 bits

Bit	Access	Default Value	Description
7:0	RW	00h	**Cache Line Size (Scratch pad):** Implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

7.8 HDR1—Header Type

B/D/F/Type: 0/6/0/PCI
Address Offset: Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access	Default Value	Description
7:0	RO	01h	**Header Type Register (HDR):** Returns 01h to indicate that this is a single function device with bridge header layout.

7.9 PBUSN1—Primary Bus Number

B/D/F/Type: 0/6/0/PCI
Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that this "virtual" Host-PCI Express bridge is connected to PCI bus #0.

Bit	Access	Default Value	Description
7:0	RO	00h	**Primary Bus Number (BUSN):** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since device #6 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0.

7.10 SBUSN1—Secondary Bus Number

B/D/F/Type: 0/6/0/PCI
Address Offset: 19h
Default Value: 00h
Access: RW
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the "virtual" bridge. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express.

Bit	Access	Default Value	Description
7:0	RW	00h	**Secondary Bus Number (BUSN):** This field is programmed by configuration software with the bus number assigned to PCI Express.

7.11 SUBUSN1—Subordinate Bus Number

B/D/F/Type: 0/6/0/PCI
Address Offset: 1Ah
Default Value: 00h
Access: RW
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express.

Bit	Access	Default Value	Description
7:0	RW	00h	**Subordinate Bus Number (BUSN):** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the device #6 bridge. When only a single PCI device resides on the PCI Express segment, this register will contain the same value as the SBUSN1 register.

7.12 IOBASE1—I/O Base Address

B/D/F/Type: 0/6/0/PCI
Address Offset: 1Ch
Default Value: F0h
Access: RO, RW
Size: 8 bits

This register controls the processor to PCI Express I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4 KB boundary.

Bit	Access	Default Value	Description
7:4	RW	Fh	**I/O Address Base (IOBASE):** This field corresponds to A[15:12] of the I/O addresses passed by bridge 1 to PCI Express.
3:0	RO	0h	Reserved

7.13 IOLIMIT1—I/O Limit Address

B/D/F/Type: 0/6/0/PCI
Address Offset: 1Dh
Default Value: 00h
Access: RW, RO
Size: 8 bits

This register controls the processor to PCI Express I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4 KB aligned address block.

Bit	Access	Default Value	Description
7:4	RW	0h	**I/O Address Limit (IOLIMIT):** Corresponds to A[15:12] of the I/O address limit of device #6. Devices between this upper limit and IOBASE1 will be passed to the PCI Express hierarchy associated with this device.
3:0	RO	0h	Reserved

7.14 SSTS1—Secondary Status

B/D/F/Type: 0/6/0/PCI
Address Offset: 1E–1Fh
Default Value: 0000h
Access: RO, RWC
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side of the "virtual" PCI-PCI bridge embedded within MCH.

Bit	Access	Default Value	Description
15	RWC	0b	**Detected Parity Error (DPE):** This bit is set by the Secondary Side for a Type 1 Configuration Space header device whenever it receives a Poisoned Transaction Layer Packet, regardless of the state of the Parity Error Response Enable bit in the Bridge Control Register.
14	RWC	0b	**Received System Error (RSE):** This bit is set when the Secondary Side for a Type 1 configuration space header device receives an ERR_FATAL or ERR_NONFATAL.
13	RWC	0b	**Received Master Abort (RMA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Unsupported Request Completion Status.
12	RWC	0b	**Received Target Abort (RTA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Completer Abort Completion Status.
11	RO	0b	**Signaled Target Abort (STA):** Not Applicable or Implemented. Hardwired to 0. The MCH does not generate Target Aborts (the MCH will never complete a request using the Completer Abort Completion status).
10:9	RO	00b	**DEVSELB Timing (DEVT):** Not Applicable or Implemented. Hardwired to 0.
8	RWC	0b	**Master Data Parity Error (SMDPE):** When set, indicates that the MCH received across the link (upstream) a Read Data Completion Poisoned Transaction Layer Packet (EP=1). This bit can only be set when the Parity Error Enable bit in the Bridge Control register is set.
7	RO	0b	**Fast Back-to-Back (FB2B):** Not Applicable or Implemented. Hardwired to 0.
6	RO	0b	Reserved
5	RO	0b	**66/60 MHz capability (CAP66):** Not Applicable or Implemented. Hardwired to 0.
4:0	RO	00h	Reserved

7.15 MBASE1—Memory Base Address

B/D/F/Type: 0/6/0/PCI
Address Offset: 20–21h
Default Value: FFF0h
Access: RW, RO
Size: 16 bits

This register controls the processor to PCI Express non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary.

Bit	Access	Default Value	Description
15:4	RW	FFFh	**Memory Address Base (MBASE):** Corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express.
3:0	RO	0h	Reserved

7.16 MLIMIT1—Memory Limit Address

B/D/F/Type: 0/6/0/PCI
Address Offset: 22–23h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

This register controls the processor to PCI Express non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1 MB aligned memory block.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI Express address ranges (typically where control/status memory-mapped I/O data structures of the controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically device local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved processor- PCI Express memory access performance.

Note: Configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges (i.e., prevent overlap with each other and/or with the ranges covered with the main memory). There is no provision in the MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not ensured.

Bit	Access	Default Value	Description
15:4	RW	000h	**Memory Address Limit (MLIMIT):** Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express.
3:0	RO	0h	Reserved

7.17 PMBASE1—Prefetchable Memory Base Address Upper

B/D/F/Type: 0/6/0/PCI
Address Offset: 24–25h
Default Value: FFF1h
Access: RW, RO
Size: 16 bits

This register in conjunction with the corresponding Upper Base Address register controls the processor to PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary.

Bit	Access	Default Value	Description
15:4	RW	FFFh	**Prefetchable Memory Base Address (MBASE):** Corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express.
3:0	RO	1h	**64-bit Address Support:** Indicates that the upper 32 bits of the prefetchable memory region base address are contained in the Prefetchable Memory base Upper Address register at 28h.

7.18 PMLIMIT1—Prefetchable Memory Limit Address

B/D/F/Type: 0/6/0/PCI
Address Offset: 26–27h
Default Value: 0001h
Access: RO, RW
Size: 16 bits

This register in conjunction with the corresponding Upper Limit Address register controls the processor to PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1 MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the processor perspective.

Bit	Access	Default Value	Description
15:4	RW	000h	**Prefetchable Memory Address Limit (PMLIMIT):** Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express.
3:0	RO	1h	**64-bit Address Support:** Indicates that the upper 32 bits of the prefetchable memory region limit address are contained in the Prefetchable Memory Base Limit Address register at 2Ch

7.19 PMBASEU1—Prefetchable Memory Base Address Upper

B/D/F/Type: 0/6/0/PCI
Address Offset: 28–2Bh
Default Value: 00000000h
Access: RW
Size: 32 bits

The functionality associated with this register is present in the PCI Express design implementation.

This register in conjunction with the corresponding Upper Base Address register controls the processor to PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary.

Bit	Access	Default Value	Description
31:0	RW	00000000h	**Prefetchable Memory Base Address (MBASEU):** Corresponds to A[63:32] of the lower limit of the prefetchable memory range that will be passed to PCI Express.

7.20 PMLIMITU1—Prefetchable Memory Limit Address Upper

B/D/F/Type: 0/6/0/PCI
Address Offset: 2C–2Fh
Default Value: 00000000h
Access: RW
Size: 32 bits

The functionality associated with this register is present in the PCI Express design implementation.

This register in conjunction with the corresponding Upper Limit Address register controls the processor to PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40- bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block.

Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the processor perspective.

Bit	Access	Default Value	Description
31:0	RW	00000000h	**Prefetchable Memory Address Limit (MLIMITU):** This field corresponds to A[63:32] of the upper limit of the prefetchable Memory range that will be passed to PCI Express.

7.21 CAPPTR1—Capabilities Pointer

B/D/F/Type: 0/6/0/PCI
Address Offset: 34h
Default Value: 88h
Access: RO
Size: 8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

Bit	Access	Default Value	Description
7:0	RO	88h	**First Capability (CAPPTR1):** The first capability in the list is the Subsystem ID and Subsystem Vendor ID Capability.

7.22 INTRLINE1—Interrupt Line

B/D/F/Type: 0/6/0/PCI
Address Offset: 3Ch
Default Value: 00h
Access: RW
Size: 8 bits

This register contains interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Bit	Access	Default Value	Description
7:0	RW	00h	**Interrupt Connection (INTCON):** Used to communicate interrupt line routing information.

7.23 INTRPIN1—Interrupt Pin

B/D/F/Type: 0/6/0/PCI
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

This register specifies which interrupt pin this device uses.

Bit	Access	Default Value	Description
7:0	RO	01h	**Interrupt Pin (INTPIN):** As a single function device, the PCI Express device specifies INTA as its interrupt pin. 01h=INTA.

7.24 BCTRL1—Bridge Control

B/D/F/Type: 0/6/0/PCI
Address Offset: 3E–3Fh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-PCI bridges. The BCTRL provides additional control for the secondary interface as well as some bits that affect the overall behavior of the "virtual" Host-PCI Express bridge embedded within MCH.

Bit	Access	Default Value	Description
15:12	RO	0h	Reserved
11	RO	0b	**Discard Timer SERR# Enable (DTSERRE):** Not Applicable or Implemented. Hardwired to 0.
10	RO	0b	**Discard Timer Status (DTSTS):** Not Applicable or Implemented. Hardwired to 0.
9	RO	0b	**Secondary Discard Timer (SDT):** Not Applicable or Implemented. Hardwired to 0.
8	RO	0b	**Primary Discard Timer (PDT):** Not Applicable or Implemented. Hardwired to 0.
7	RO	0b	**Fast Back-to-Back Enable (FB2BEN):** Not Applicable or Implemented. Hardwired to 0.
6	RW	0b	**Secondary Bus Reset (SRESET):** Setting this bit triggers a hot reset on the corresponding PCI Express Port. This will force the LTSSM to transition to the Hot Reset state (via Recovery) from L0 or L1 states.
5	RO	0b	**Master Abort Mode (MAMODE):** Does not apply to PCI Express. Hardwired to 0.
4	RW	0b	**VGA 16-bit Decode (VGA16D):** Enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if bit 3 (VGA Enable) of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. 0 = Execute 10-bit address decodes on VGA I/O accesses. 1 = Execute 16-bit address decodes on VGA I/O accesses.
3	RW	0b	**VGA Enable (VGAEN):** Controls the routing of processor initiated transactions targeting VGA compatible I/O and memory address ranges. See the VGAEN/MDAP table in device 0, offset 97h[0].
2	RW	0b	**ISA Enable (ISAEN):** Needed to exclude legacy resource decode to route ISA resources to legacy decode path. Modifies the response by the MCH to an I/O access issued by the processor that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions will be mapped to PCI Express. 1 = MCH will not forward to PCI Express any I/O transactions addressing the last 768 bytes in each 1 KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers.

Bit	Access	Default Value	Description
1	RW	0b	**SERR Enable (SERREN):** 0 = No forwarding of error messages from secondary side to primary side that could result in an SERR. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.
0	RW	0b	**Parity Error Response Enable (PEREN):** Controls whether or not the Master Data Parity Error bit in the Secondary Status register is set when the MCH receives across the link (upstream) a Read Data Completion Poisoned Transaction Layer Packet. 0 = Master Data Parity Error bit in Secondary Status register can NOT be set. 1 = Master Data Parity Error bit in Secondary Status register CAN be set.

7.25 PM_CAPID1—Power Management Capabilities

B/D/F/Type: 0/6/0/PCI
Address Offset: 80–83h
Default Value: C8039001h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:27	RO	19h	**PME Support (PMES):** This field indicates the power states in which this device may indicate PME wake via PCI Express messaging. D0, D3hot & D3cold. This device is not required to do anything to support D3hot and D3cold, it simply must report that those states are supported. Refer to the PCI Power Management 1.1 specification for encoding explanation and other power management details.
26	RO	0b	**D2 Power State Support (D2PSS):** Hardwired to 0 to indicate that the D2 power management state is NOT supported.
25	RO	0b	**D1 Power State Support (D1PSS):** Hardwired to 0 to indicate that the D1 power management state is NOT supported.
24:22	RO	000b	**Auxiliary Current (AUXC):** Hardwired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.
21	RO	0b	**Device Specific Initialization (DSI):** Hardwired to 0 to indicate that special initialization of this device is NOT required before generic class device driver is to use it.
20	RO	0b	**Auxiliary Power Source (APS):** Hardwired to 0.
19	RO	0b	**PME Clock (PMECLK):** Hardwired to 0 to indicate this device does NOT support PMEB generation.
18:16	RO	011b	**PCI PM CAP Version (PCIPMCV):** A value of 011b indicates that this function complies with revision 1.2 of the PCI Power Management Interface Specification.
15:8	RO	90h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, then the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h.
7:0	RO	01h	**Capability ID (CID):** Value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.

7.26 PM_CS1—Power Management Control/Status

B/D/F/Type: 0/6/0/PCI
Address Offset: 84–87h
Default Value: 00000008h
Access: RO, RW, RW/P
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	Reserved
15	RO	0b	**PME Status (PMESTS):** Indicates that this device does not support PMEB generation from D3cold.
14:13	RO	00b	**Data Scale (DSCALE):** Indicates that this device does not support the power management data register.
12:9	RO	0h	**Data Select (DSEL):** Indicates that this device does not support the power management data register.
8	RW/P	0b	**PME Enable (PMEE):** Indicates that this device does not generate PMEB assertion from any D-state. 0 = PMEB generation not possible from any D State 1 = PMEB generation enabled from any D State The setting of this bit has no effect on hardware. See PM_CAP[15:11]
7:2	RO	0000b	Reserved
1:0	RW	00b	**Power State (PS):** Indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00 = D0 01 = D1 (Not supported in this device.) 10 = D2 (Not supported in this device.) 11 = D3 Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state in order to be fully-functional. When the Power State is other than D0, the bridge will Master Abort (i.e. not claim) any downstream cycles (with exception of type 0 config cycles). Consequently, these unclaimed cycles will go down DMI and come back up as Unsupported Requests, which the MCH logs as Master Aborts in Device 0 PCISTS[13] There is no additional hardware functionality required to support these Power States.

7.27 SS_CAPID—Subsystem ID and Vendor ID Capabilities

B/D/F/Type: 0/6/0/PCI
Address Offset: 88–8Bh
Default Value: 0000800Dh
Access: RO
Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides. Because this device is an integrated part of the system and not an add-in device, it is anticipated that this capability will never be used. However, it is necessary because Microsoft will test for its presence.

Bit	Access	Default Value	Description
31:16	RO	0000h	Reserved
15:8	RO	80h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list which is the PCI Power Management capability.
7:0	RO	0Dh	**Capability ID (CID):** Value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI Bridge.

7.28 SS—Subsystem ID and Subsystem Vendor ID

B/D/F/Type: 0/6/0/PCI
Address Offset: 8C–8Fh
Default Value: 00008086h
Access: RWO
Size: 32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and a hardware reset.

Bit	Access	Default Value	Description
31:16	RWO	0000h	**Subsystem ID (SSID):** Identifies the particular subsystem and is assigned by the vendor.
15:0	RWO	8086h	**Subsystem Vendor ID (SSVID):** Identifies the manufacturer of the subsystem and is the same as the vendor ID which is assigned by the PCI Special Interest Group.

7.29 MSI_CAPID—Message Signaled Interrupts Capability ID

B/D/F/Type: 0/6/0/PCI
Address Offset: 90–91h
Default Value: A005h
Access: RO
Size: 16 bits

When a device supports MSI, it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

Bit	Access	Default Value	Description
15:8	RO	A0h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list which is the PCI Express capability.
7:0	RO	05h	**Capability ID (CID):** Value of 05h identifies this linked list item (capability structure) as being for MSI registers.

7.30 MC—Message Control

B/D/F/Type: 0/6/0/PCI
Address Offset: 92–93h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so.

If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access	Default Value	Description
15:8	RO	00h	Reserved
7	RO	0b	**64-bit Address Capable (64AC):** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address.
6:4	RW	000b	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
3:1	RO	000b	**Multiple Message Capable (MMC):** System software reads this field to determine the number of messages being requested by this device. The value of 000b equates to 1 message requested. 000 = 1 message requested All other encodings are reserved.
0	RW	0b	**MSI Enable (MSIEN):** Controls the ability of this device to generate MSIs. 0 = MSI will not be generated. 1 = MSI will be generated when we receive PME messages. INTA will not be generated and INTA Status (PCISTS1[3]) will not be set.

7.31 MA—Message Address

B/D/F/Type: 0/6/0/PCI
Address Offset: 94–97h
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

Bit	Access	Default Value	Description
31:2	RW	00000000h	**Message Address (MA):** Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO	00b	**Force DWord Align (FDWA):** Hardwired to 0 so that addresses assigned by system software are always aligned on a DWord address boundary.

7.32 MD—Message Data

B/D/F/Type: 0/6/0/PCI
Address Offset: 98–99h
Default Value: 0000h
Access: RW
Size: 16 bits

Bit	Access	Default Value	Description
15:0	RW	0000h	**Message Data (MD):** Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16-bits are always set to 0. The lower 16-bits are supplied by this register.

7.33 PE_CAPL—PCI Express* Capability List

B/D/F/Type: 0/6/0/PCI
Address Offset: A0–A1h
Default Value: 0010h
Access: RO
Size: 16 bits

This register enumerates the PCI Express capability structure.

Bit	Access	Default Value	Description
15:8	RO	00h	**Pointer to Next Capability (PNC):** This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express Extended Configuration Space.
7:0	RO	10h	**Capability ID (CID):** Identifies this linked list item (capability structure) as being for PCI Express registers.

7.34 PE_CAP—PCI Express* Capabilities

B/D/F/Type: 0/6/0/PCI
Address Offset: A2–A3h
Default Value: 0142h
Access: RO, RWO
Size: 16 bits

This register indicates PCI Express device capabilities.

Bit	Access	Default Value	Description
15:14	RO	00b	Reserved
13:9	RO	00h	**Interrupt Message Number (IMN):** Not Applicable or Implemented. Hardwired to 0.
8	RWO	1b	**Slot Implemented (SI):** 0 = The PCI Express Link associated with this port is connected to an integrated component or is disabled. 1 = The PCI Express Link associated with this port is connected to a slot.
7:4	RO	4h	**Device/Port Type (DPT):** Hardwired to 4h to indicate root port of PCI Express Root Complex.
3:0	RO	2h	**PCI Express Capability Version (PCIECV):** Hardwired to 2h to indicate compliance to the PCI Express Capabilities Register Expansion ECN.

7.35 DCAP—Device Capabilities

B/D/F/Type: 0/6/0/PCI
Address Offset: A4–A7h
Default Value: 00008000h
Access: RO
Size: 32 bits

This register indicates PCI Express device capabilities.

Bit	Access	Default Value	Description
31:16	RO	0000h	Reserved
15	RO	1b	**Role Based Error Reporting (RBER):** This bit indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 1.1 specification.
14:6	RO	000h	Reserved
5	RO	0b	**Extended Tag Field Supported (ETFS):** Hardwired to indicate support for 5-bit Tags as a Requestor.
4:3	RO	00b	**Phantom Functions Supported (PFS):** Not Applicable or Implemented. Hardwired to 0.
2:0	RO	000b	**Max Payload Size (MPS):** Hardwired to indicate 128B max supported payload for Transaction Layer Packets (TLP).

7.36 DCTL—Device Control

B/D/F/Type: 0/6/0/PCI
Address Offset: A8–A9h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

This register provides control for PCI Express device specific capabilities.

The error reporting enable bits are in reference to errors detected by this device, not error messages received across the link. The reporting of error messages (ERR_CORR, ERR_NONFATAL, ERR_FATAL) received by Root Port is controlled exclusively by Root Port Command Register.

Bit	Access	Default Value	Description
15:8	RO	0h	Reserved
7:5	RW	000b	**Max Payload Size (MPS):** 000 = 128B max supported payload for Transaction Layer Packets (TLP). As a receiver, the Device must handle TLPs as large as the set value; as transmitter, the Device must not generate TLPs exceeding the set value. All other encodings are reserved. Hardware will actually ignore this field. It is writeable only to support compliance testing.
4	RO	0b	Reserved
3	RW	0b	**Unsupported Request Reporting Enable (URRE):** When set, this bit allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_CORR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_CORR is signaled when an unmasked Advisory Non-Fatal UR is received. An ERR_FATAL or ERR_NONFATAL is sent to the Root Control register when an uncorrectable non-Advisory UR is received with the severity bit set in the Uncorrectable Error Severity register.
2	RW	0b	**Fatal Error Reporting Enable (FERE):** When set, this bit enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	RW	0b	**Non-Fatal Error Reporting Enable (NERE):** When set, this bit enables signaling of ERR_NONFATAL to the Rool Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	RW	0b	**Correctable Error Reporting Enable (CERE):** When set, this bit enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

7.37 DSTS—Device Status

B/D/F/Type: 0/6/0/PCI
Address Offset: AA–ABh
Default Value: 0000h
Access: RO, RWC
Size: 16 bits

This register reflects status corresponding to controls in the Device Control register. The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

Bit	Access	Default Value	Description
15:6	RO	000h	Reserved
5	RO	0b	**Transactions Pending (TP):** 0 = All pending transactions (including completions for any outstanding non-posted requests on any used virtual channel) have been completed. 1 = Indicates that the device has transaction(s) pending (including completions for any outstanding non-posted requests for all used Traffic Classes).
4	RO	0b	Reserved
3	RWC	0b	**Unsupported Request Detected (URD):** When set, this bit indicates that the Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register. Additionally, the Non-Fatal Error Detected bit or the Fatal Error Detected bit is set according to the setting of the Unsupported Request Error Severity bit. In production systems setting the Fatal Error Detected bit is not an option as support for AER will not be reported.
2	RWC	0b	**Fatal Error Detected (FED):** When set, this bit indicates that fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
1	RWC	0b	**Non-Fatal Error Detected (NFED):** When set, this bit indicates that non-fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
0	RWC	0b	**Correctable Error Detected (CED):** When set, this bit indicates that correctable error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the correctable error mask register.

7.38 LCAP—Link Capabilities

B/D/F/Type: 0/6/0/PCI
Address Offset: AC–AFh
Default Value: 03214D02h
Access: RO, RWO
Size: 32 bits

This register indicates PCI Express device specific capabilities.

Bit	Access	Default Value	Description
31:24	RO	03h	**Port Number (PN):** This field indicates the PCI Express port number for the given PCI Express link. Matches the value in Element Self Description[31:24].
23:22	RO	000b	Reserved
21	RO	1b	**Link Bandwidth Notification Capability:** A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. This capability is required for all Root Ports and Switch downstream ports supporting Links wider than x1 and/or multiple Link speeds. This field is not applicable and is reserved for Endpoint devices, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Devices that do not implement the Link Bandwidth Notification capability must hardwire this bit to 0b.
20	RO	0b	**Data Link Layer Link Active Reporting Capable (DLLLARC):** For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.
19	RO	0b	**Surprise Down Error Reporting Capable (SDERC):** For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.
18	RO	0b	**Clock Power Management (CPM):** A value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) when the link is in the L1 and L2/3 Ready link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these link states. This capability is applicable only in form factors that support "clock request" (CLKREQ#) capability. For a multi-function device, each function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the multifunction device indicate a 1b in this bit.
17:15	RWO	010b	**L1 Exit Latency (L1ELAT):** Indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010 b indicates the range of 2 us to less than 4 us. Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.
14:12	RO	100b	Reserved
11:10	RWO	11b	**Active State Link PM Support (ASLPMS)::** The MCH supports ASPM L1.

Bit	Access	Default Value	Description
9:4	RO	10h	**Max Link Width (MLW):** Indicates the maximum number of lanes supported for this link. 10h = x16
3:0	RO	2h	**Max Link Speed (MLS):** Supported Link Speed - This field indicates the supported Link speed(s) of the associated Port. 0001b = 2.5GT/s Link speed supported 0010b = 5.0GT/s and 2.5GT/s Link speeds supported All other encodings are reserved.

7.39 LCTL—Link Control

B/D/F/Type: 0/6/0/PCI
Address Offset: B0–B1h
Default Value: 0000h
Access: RO, RW, RW/SC
Size: 16 bits

This register allows control of PCI Express link.

Bit	Access	Default Value	Description
15:12	RO	0000000b	Reserved
11	RW	0b	**Link Autonomous Bandwidth Interrupt Enable:** When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set. This bit is not applicable and is reserved for Endpoint devices, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Devices that do not implement the Link Bandwidth Notification capability must hardwire this bit to 0b.
10	RW	0b	**Link Bandwidth Management Interrupt Enable:** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set. This bit is not applicable and is reserved for Endpoint devices, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches.
9	R0	0b	**Hardware Autonomous Width Disable:** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Devices that do not implement the ability autonomously to change Link width are permitted to hardwire this bit to 0b. The MCH does not support autonomous width change. So, this bit is "RO".
8	RO	0b	**Enable Clock Power Management (ECPM):** Applicable only for form factors that support a "Clock Request" (CLKREQ#) mechanism, this enable functions as follows: 0 = Clock power management is disabled and device must hold CLKREQ# signal low 1 = The device is permitted to use CLKREQ# signal to power manage link clock according to protocol defined in appropriate form factor specification. Default value of this field is 0b. Components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities Register) must hardwire this bit to 0b.
7	RW	0b	**Extended Synch (ES):** 0 = Standard Fast Training Sequence (FTS). 1 = Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state. This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and symbol lock before the link enters L0 and resumes communication. This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns. **NOTE:** The 82X48 MCH does not support L0s.

Bit	Access	Default Value	Description
6	RW	0b	**Common Clock Configuration (CCC):** 0 = Indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. 1 = Indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock.
5	RW/SC	0b	**Retrain Link (RL):** 0 = Normal operation. 1 = Full Link retraining is initiated by directing the Physical Layer LTSSM from L0 or L1 states to the Recovery state. This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0). It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	RW	0b	**Link Disable (LD):** 0 = Normal operation. 1 = Link is disabled. Forces the LTSSM to transition to the Disabled state (via Recovery) from L0 or L1 states. Link retraining happens automatically on 0 to 1 transition, just like when coming out of reset. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.
3	RO	0b	**Read Completion Boundary (RCB):** Hardwired to 0 to indicate 64 byte.
2	RW	0b	Reserved
1:0	RW	00b	**Active State PM (ASPM):** Controls the level of active state power management supported on the given link. 00 = Disabled 01 = Reserved 10 = Reserved 11 = L1 Entry Supported

7.40 LSTS—Link Status

B/D/F/Type: 0/6/0/PCI
Address Offset: B2–B3h
Default Value: 1000h
Access: RWC, RO
Size: 16 bits

This register indicates PCI Express link status.

Bit	Access	Default Value	Description
15	RWC	0b	**Link Autonomous Bandwidth Status (LABWS):** This bit is set to 1b by hardware to indicate that hardware has autonomously changed link speed or width, without the port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the downstream component that was indicated as an autonomous change.
14	RWC	0b	**Link Bandwidth Management Status (LBWMS):** This bit is set to 1b by hardware to indicate that either of the following has occurred without the port transitioning through DL_Down status: A link retraining initiated by a write of 1b to the Retrain Link bit has completed. **NOTE:** This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. Hardware has autonomously changed link speed or width to attempt to correct unreliable link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the downstream component that was not indicated as an autonomous change.
13	RO	0b	**Data Link Layer Link Active (Optional) (DLLLA):** This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. This bit must be implemented if the corresponding Data Link Layer Active Capability bit is implemented. Otherwise, this bit must be hardwired to 0b.
12	RO	1b	**Slot Clock Configuration (SCC):** 0 = The device uses an independent clock irrespective of the presence of a reference on the connector. 1 = The device uses the same physical reference clock that the platform provides on the connector.
11	RO	0b	**Link Training (LTRN):** This bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state once Link training is complete.
10	RO	0b	**Undefined:** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.

Bit	Access	Default Value	Description
9:4	RO	00h	**Negotiated Link Width (NLW):** Indicates negotiated link width. This field is valid only when the link is in the L0 or L1 states (after link width negotiation is successfully completed). 01h = x1 04h = ‘x4 — This is not a supported PCIe Gen2.0 link width. Link width x4 is only valid when PCIe Gen1.1 I/O card is used in the secondary port. 08h = x8 — This is not a supported PCIe Gen2.0 link width. Link width x8 is only valid when PCIe Gen1.1 I/O card is used in the secondary port. 10h = x16 All other encodings are reserved.
3:0	RO	0h	**Current Link Speed (CLS):** This field indicates the negotiated Link speed of the given PCI Express Link. Defined encodings are: 0001b = 5.0 GT/s PCI Express Link 0010b = 5 GT/s PCI Express Link All other encodings are reserved. The value in this field is undefined when the Link is not up.

7.41 SLOTCAP—Slot Capabilities

B/D/F/Type: 0/6/0/PCI
Address Offset: B4–B7h
Default Value: 00040000h
Access: RWO, RO
Size: 32 bits

PCI Express Slot related registers.

Bit	Access	Default Value	Description
31:19	RWO	0000h	**Physical Slot Number (PSN):** Indicates the physical slot number attached to this Port.
18	RO	1b	Reserved
17	RO	0b	**Electromechanical Interlock Present (EIP):** When set to 1b, this bit indicates that an Electromechanical Interlock is implemented on the chassis for this slot.
16:15	RWO	00b	**Slot Power Limit Scale (SPLS):** Specifies the scale used for the Slot Power Limit Value. 00 = 1.0x 01 = 0.1x 10 = 0.01x 11 = 0.001x If this field is written, the link sends a Set_Slot_Power_Limit message.
14:7	RWO	00h	**Slot Power Limit Value (SPLV):** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. If this field is written, the link sends a Set_Slot_Power_Limit message.

Bit	Access	Default Value	Description
6:5	RO	00b	Reserved
4	RO	0b	**Power Indicator Present (PIP):** When set to 1b, this bit indicates that a Power Indicator is electrically controlled by the chassis for this slot.
3	RO	0b	**Attention Indicator Present (AIP):** When set to 1b, this bit indicates that an Attention Indicator is electrically controlled by the chassis.
2	RO	0b	**MRL Sensor Present (MSP):** When set to 1b, this bit indicates that an MRL Sensor is implemented on the chassis for this slot.
1	RO	0b	**Power Controller Present (PCP):** When set to 1b, this bit indicates that a software programmable Power Controller is implemented for this slot/adapter (depending on form factor).
0	RO	0b	**Attention Button Present (ABP):** When set to 1b, this bit indicates that an Attention Button for this slot is electrically controlled by the chassis.

7.42 SLOTCTL—Slot Control

B/D/F/Type: 0/6/0/PCI
Address Offset: B8–B9h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

PCI Express Slot related registers.

Bit	Access	Default Value	Description
15:13	RO	000b	Reserved
12	RO	0b	**Data Link Layer State Changed Enable (DLLSCE):** If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed. If the Data Link Layer Link Active capability is not implemented, this bit is permitted to be read-only with a value of 0b.
11	RO	0b	**Electromechanical Interlock Control (EIC):** If an Electromechanical Interlock is implemented, a write of 1b to this field causes the state of the interlock to toggle. A write of 0b to this field has no effect. A read to this register always returns a 0.
10	RO	0b	**Power Controller Control (PCC):** If a Power Controller is implemented, this field when written sets the power state of the slot per the defined encodings. Reads of this field must reflect the value from the latest write, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. Depending on the form factor, the power is turned on/off either to the slot or within the adapter. Note that in some cases the power controller may autonomously remove slot power or not respond to a power-up request based on a detected fault condition, independent of the Power Controller Control setting. 0 = Power On 1 = Power Off If the Power Controller Implemented field in the Slot Capabilities register is set to 0b, then writes to this field have no effect and the read value of this field is undefined.

Bit	Access	Default Value	Description
9:8	RO	00b	**Power Indicator Control (PIC):** If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 00 = Reserved 01 = On 10 = Blink 11 = Off If the Power Indicator Present bit in the Slot Capabilities register is 0b, this field is permitted to be read-only with a value of 00b.
7:6	RO	00b	**Attention Indicator Control (AIC):** If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Reads of this field must reflect the value from the latest write, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. If the indicator is electrically controlled by chassis, the indicator is controlled directly by the downstream port through implementation specific mechanisms. 00 = Reserved 01 = On 10 = Blink 11 = Off If the Attention Indicator Present bit in the Slot Capabilities register is 0b, this field is permitted to be read only with a value of 00b.
5:4	RO	00b	Reserved
3	RW	0b	**Presence Detect Changed Enable (PDCE):** When set to 1b, this bit enables software notification on a presence detect changed event.
2	RO	0b	**MRL Sensor Changed Enable (MSCE):** When set to 1b, this bit enables software notification on a MRL sensor changed event. Default value of this field is 0b. If the MRL Sensor Present field in the Slot Capabilities register is set to 0b, this bit is permitted to be read-only with a value of 0b.
1	RO	0b	**Power Fault Detected Enable (PFDE):** When set to 1b, this bit enables software notification on a power fault event. Default value of this field is 0b. If Power Fault detection is not supported, this bit is permitted to be read-only with a value of 0b
0	RO	0b	**Button Pressed Enable (ABPE):** When set to 1b, this bit enables software notification on an attention button pressed event.

7.43 SLOTSTS—Slot Status

B/D/F/Type: 0/6/0/PCI
Address Offset: BA–BBh
Default Value: 0000h
Access: RO, RWC
Size: 16 bits

PCI Express Slot related registers.

Bit	Access	Default Value	Description
15:7	RO	0000000b	Reserved
6	RO	0b	**Presence Detect State (PDS):** This bit indicates the presence of an adapter in the slot, reflected by the logical "OR" of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. 0 = Slot Empty 1 = Card Present in Slot This register must be implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities Register is 0b), this bit must return 1b.
5:4	RO	00b	Reserved
3	RWC	0b	**Detect Changed (PDC):** This bit is set when the value reported in Presence Detect State is changed.
2	RO	0b	**MRL Sensor Changed (MSC):** If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be set.
1	RO	0b	**Power Fault Detected (PFD):** If a Power Controller that supports power fault detection is implemented, this bit is set when the Power Controller detects a power fault at this slot. Note that, depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be set.
0	RO	0b	**Attention Button Pressed (ABP):** If an Attention Button is implemented, this bit is set when the attention button is pressed. If an Attention Button is not supported, this bit must not be set.

7.44 RCTL—Root Control

B/D/F/Type: 0/6/0/PCI
Address Offset: BC–BDh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when our device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR as controlled by these bits takes precedence over the SERR Enable in the PCI Command Register.

Bit	Access	Default Value	Description
15:4	RO	000h	Reserved
3	RW	0b	**PME Interrupt Enable (PMEIE):** 0 = No interrupts are generated as a result of receiving PME messages. 1 = Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status Register. A PME interrupt is also generated if the PME Status bit of the Root Status Register is set when this bit is set from a cleared state.
2	RW	0b	**System Error on Fatal Error Enable (SEFEE):** Controls the Root Complex's response to fatal errors. 0 = No SERR generated on receipt of fatal error. 1 = Indicates that an SERR should be generated if a fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
1	RW	0b	**System Error on Non-Fatal Uncorrectable Error Enable (SENFUEE):** Controls the Root Complex's response to non-fatal errors. 0 = No SERR generated on receipt of non-fatal error. 1 = Indicates that an SERR should be generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
0	RW	0b	**System Error on Correctable Error Enable (SECEE):** Controls the Root Complex's response to correctable errors. 0 = No SERR generated on receipt of correctable error. 1 = Indicates that an SERR should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.

7.45 RSTS—Root Status

B/D/F/Type: 0/6/0/PCI
Address Offset: C0–C3h
Default Value: 00000000h
Access: RO, RWC
Size: 32 bits

This register provides information about PCI Express Root Complex specific parameters.

Bit	Access	Default Value	Description
31:18	RO	0000h	Reserved
17	RO	0b	**PME Pending (PMEP):** Indicates that another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16	RWC	0b	**PME Status (PMES):** Indicates that PME was asserted by the requestor ID indicated in the PME Requestor ID field. Subsequent PMEs are kept pending until the status register is cleared by writing a 1 to this field.
15:0	RO	0000h	**PME Requestor ID (PMERID):** Indicates the PCI requestor ID of the last PME requestor.

7.46 PELC—PCI Express Legacy Control

B/D/F/Type: 0/6/0/PCI
Address Offset: EC–EFh
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

This register controls functionality that is needed by Legacy (non-PCI Express aware) OSs during run time.

Bit	Access	Default Value	Description
31:3	RO	0000000 0h	Reserved
2	RW	0b	**PME GPE Enable (PMEGPE):** 0 = Do not generate GPE PME message when PME is received. 1 = Generate a GPE PME message when PME is received (Assert_PMEGPE and Deassert_PMEGPE messages on DMI). This enables the MCH to support PMEs on the PCI Express port under legacy OSs.
1	RO	0b	Reserved
0	RW	0b	**General Message GPE Enable (GENGPE):** 0 = Do not forward received GPE assert/de-assert messages. 1 = Forward received GPE assert/de-assert messages. These general GPE message can be received via the PCI Express port from an external Intel device and will be subsequently forwarded to the ICH (via Assert_GPE and Deassert_GPE messages on DMI).

7.47 VCECH—Virtual Channel Enhanced Capability Header

B/D/F/Type: 0/6/0/MMR
Address Offset: 100–103h
Default Value: 14010002h
Access: RO
Size: 32 bits

This register indicates PCI Express device Virtual Channel capabilities. Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

Bit	Access	Default Value	Description
31:20	RO	140h	**Pointer to Next Capability (PNC):** The Link Declaration Capability is the next in the PCI Express extended capabilities list.
19:16	RO	1h	**PCI Express Virtual Channel Capability Version (PCIEVCCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. Note: This version does not change for 2.0 compliance.
15:0	RO	0002h	**Extended Capability ID (ECID):** Value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

7.48 PVCCAP1—Port VC Capability Register 1

B/D/F/Type: 0/6/0/MMR
Address Offset: 104–107h
Default Value: 00000000h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:7	RO	00000h	Reserved
6:4	RO	000b	**Low Priority Extended VC Count (LPEVCC):** This field indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO	0b	Reserved
2:0	RO	000b	**Extended VC Count (EVCC):** This field indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

7.49 PVCCAP2—Port VC Capability Register 2

B/D/F/Type: 0/6/0/MMR
Address Offset: 108–10Bh
Default Value: 00000000h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:24	RO	00h	**VC Arbitration Table Offset (VCATO):** This field indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Capability Structure. A value of 0 indicates that the table is not present (due to fixed VC priority).
23:0	RO	0000h	Reserved

7.50 PVCCTL—Port VC Control

B/D/F/Type: 0/6/0/MMR
Address Offset: 10C–10Dh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

Bit	Access	Default Value	Description
15:4	RO	000h	Reserved
3:1	RW	000b	**VC Arbitration Select (VCAS):** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. Since there is no other VC supported than the default, this field is reserved.
0	RO	0b	Reserved

7.51 VC0RCAP—VC0 Resource Capability

B/D/F/Type: 0/6/0/MMR
Address Offset: 110–113h
Default Value: 00000001h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0000h	Reserved
15	RO	0b	**Reject Snoop Transactions (RSNPT):** 0 = Transactions with or without the No Snoop bit set within the Transaction Layer Packet header are allowed on this VC. 1 = When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
14:8	RO	0000h	Reserved
7:0	RO	01h	**Port Arbitration Capability:** Indicates types of Port Arbitration supported by the VC resource. This field is valid for all Switch Ports, Root Ports that support peer-to-peer traffic, and RCRBs, but not for PCI Express Endpoint devices or Root Ports that do not support peer to peer traffic. Each bit location within this field corresponds to a Port Arbitration Capability defined below. When more than one bit in this field is Set, it indicates that the VC resource can be configured to provide different arbitration services. Software selects among these capabilities by writing to the Port Arbitration Select field (see below). Bit[0] = Default = 01b; Non-configurable hardware-fixed arbitration scheme, e.g., Round Robin (RR) Bit[1] = Weighted Round Robin (WRR) arbitration with 32 phases Bit[2] = WRR arbitration with 64 phases Bit[3] = WRR arbitration with 128 phases Bit[4] = Time-based WRR with 128 phases Bit[5] = WRR arbitration with 256 phases Bits[6:7] = Reserved MCH default indicates "Non-configurable hardware-fixed arbitration scheme".

7.52 VC0RCTL—VC0 Resource Control

B/D/F/Type: 0/6/0/MMR
Address Offset: 114–117h
Default Value: 800000FFh
Access: RO, RW
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access	Default Value	Description
31	RO	1b	**VC0 Enable (VC0E):** For VC0, this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO	0h	Reserved
26:24	RO	000b	**VC0 ID (VC0ID):** This field assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:20	RO	0000h	Reserved
19:17	RW	000b	**Port Arbitration Select:** This field configures the VC resource to provide a particular Port Arbitration service. This field is valid for RCRBs, Root Ports that support peer to peer traffic, and Switch Ports, but not for PCI Express Endpoint devices or Root Ports that do not support peer to peer traffic. The permissible value of this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource.
16:8	RO	00h	Reserved
7:1	RW	7Fh	**TC/VC0 Map (TCVC0M):** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. To remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	1b	**TC0/VC0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.

7.53 VC0RSTS—VC0 Resource Status

B/D/F/Type: 0/6/0/MMR
Address Offset: 11A–11Bh
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	Reserved
1	RO	1b	**VC0 Negotiation Pending (VC0NP):** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	Reserved

7.54 RCLDECH—Root Complex Link Declaration Enhanced

B/D/F/Type: 0/6/0/MMR
Address Offset: 140–143h
Default Value: 00010005h
Access: RO
Size: 32 bits

This capability declares links from this element (PCI Express) to other elements of the root complex component to which it belongs. See PCI Express specification for link/ topology declaration requirements.

Bit	Access	Default Value	Description
31:20	RO	000h	**Pointer to Next Capability (PNC):** This is the last capability in the PCI Express extended capabilities list.
19:16	RO	1h	**Link Declaration Capability Version (LDCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. Note: This version does not change for 2.0 compliance.
15:0	RO	0005h	**Extended Capability ID (ECID):** Value of 0005h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

7.55 ESD—Element Self Description

B/D/F/Type: 0/6/0/MMR
Address Offset: 144–147h
Default Value: 03000100h
Access: RO, RWO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access	Default Value	Description
31:24	RO	03h	**Port Number (PN):** This field specifies the port number associated with this element with respect to the component that contains this element. This port number value is used by the egress port of the component to provide arbitration to this Root Complex Element.
23:16	RWO	00h	**Component ID (CID):** This field indicates the physical component that contains this Root Complex Element.
15:8	RO	01h	**Number of Link Entries (NLE):** This field indicates the number of link entries following the Element Self Description. This field reports 1 (to Egress port only as we don't report any peer-to-peer capabilities in our topology).
7:4	RO	0h	Reserved
3:0	RO	0h	**Element Type (ET):** This field indicates Configuration Space Element.

7.56 LE1D—Link Entry 1 Description

B/D/F/Type: 0/6/0/MMR
Address Offset: 150–153h
Default Value: 00000000h
Access: RO, RWO
Size: 32 bits

This register provides the first part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
31:24	RO	00h	**Target Port Number (TPN):** This field specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	RWO	00h	**Target Component ID (TCID):** This field identifies the physical or logical component that is targeted by this link entry.
15:2	RO	0000h	Reserved
1	RO	0b	**Link Type (LTYP):** This bit indicates that the link points to memory–mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	RWO	0b	**Link Valid (LV):** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

7.57 LE1A—Link Entry 1 Address

B/D/F/Type: 0/6/0/MMR
Address Offset: 158–15Fh
Default Value: 0000000000000000h
Access: RO, RWO
Size: 64 bits

This register provides the second part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access	Default Value	Description
63:32	RO	0000000 0h	Reserved
31:12	RWO	00000h	**Link Address (LA):** This field provides the memory mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0	RO	000h	Reserved

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8 Direct Media Interface (DMI) RCRB

This Root Complex Register Block (RCRB) controls the MCH-ICH9 serial interconnect. The base address of this space is programmed in DMIBAR in D0:F0 configuration space. Table 14 provides an address map of the DMI registers listed by address offset in ascending order.

Note: IMPORTANT: All RCRB register space needs to remain organized as shown here.

Table 14. Direct Media Interface Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
0–3h	DMIVCECH	DMI Virtual Channel Enhanced Capability	04010002h	RO
4–7h	DMIPVCCAP1	DMI Port VC Capability Register 1	00000001h	RWO, RO
C–Dh	DMIPVCCTL	DMI Port VC Control	0000h	RO, RW
10–13h	DMIVC0RCAP	DMI VC0 Resource Capability	00000001h	RO
14–17h	DMIVC0RCTL0	DMI VC0 Resource Control	800000FFh	RO, RW
1A–1Bh	DMIVC0RSTS	DMI VC0 Resource Status	0002h	RO
1C–1Fh	DMIVC1RCAP	DMI VC1 Resource Capability	00008001h	RO
20–23h	DMIVC1RCTL1	DMI VC1 Resource Control	01000000h	RW, RO
26–27h	DMIVC1RSTS	DMI VC1 Resource Status	0002h	RO
84–87h	DMILCAP	DMI Link Capabilities	00012C41h	RO, RWO
88–89h	DMILCTL	DMI Link Control	0000h	RW, RO
8A–8Bh	DMILSTS	DMI Link Status	0001h	RO

8.1 DMIVCECH—DMI Virtual Channel Enhanced Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 0–3h
Default Value: 04010002h
Access: RO
Size: 32 bits

This register indicates DMI Virtual Channel capabilities.

Bit	Access	Default Value	Description
31:20	RO	040h	**Pointer to Next Capability (PNC):** This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Link Declaration Capability).
19:16	RO	1h	**PCI Express Virtual Channel Capability Version (PCIEVCCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. Note: This version does not change for 2.0 compliance.
15:0	RO	0002h	**Extended Capability ID (ECID):** Value of 0002 h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

8.2 DMIPVCCAP1—DMI Port VC Capability Register 1

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 4–7h
Default Value: 00000001h
Access: RWO, RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
31:7	RO	0000000h	Reserved
6:4	RO	000b	**Low Priority Extended VC Count (LPEVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO	0b	Reserved
2:0	RWO	001b	**Extended VC Count (EVCC):** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. The Private Virtual Channel is not included in this count.

8.3 DMIPVCCTL—DMI Port VC Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: C–Dh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

Bit	Access	Default Value	Description
15:4	RO	000h	Reserved
3:1	RW	000b	**VC Arbitration Select (VCAS):** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. See the PCI express specification for more details
0	RO	0b	Reserved

8.4 DMIVC0RCAP—DMI VC0 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 10–13h
Default Value: 00000001h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	0s	Reserved
15	RO	0b	**Reject Snoop Transactions (REJSNPT):** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
14:8	RO	00h	Reserved
7:0	RO	01h	**Port Arbitration Capability (PAC):** Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

8.5 DMIVC0RCTL0—DMI VC0 Resource Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 14–17h
Default Value: 800000FFh
Access: RO, RW
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access	Default Value	Description
31	RO	1b	**Virtual Channel 0 Enable (VC0E):** For VC0, this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO	0h	Reserved
26:24	RO	000b	**Virtual Channel 0 ID (VC0ID):** Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:20	RO	0h	Reserved
19:17	RW	000b	**Port Arbitration Select (PAS):** This field configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource. Because only bit 0 of that field is asserted. This field will always be programmed to 1.
16:8	RO	000h	Reserved
7:1	RW	7Fh	**Traffic Class / Virtual Channel 0 Map (TCVC0M):** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	1b	**Traffic Class 0 / Virtual Channel 0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.

8.6 DMIVC0RSTS—DMI VC0 Resource Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 1A–1Bh
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	Reserved
1	RO	1b	**Virtual Channel 0 Negotiation Pending (VC0NP):** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. **BIOS Requirement:** Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO	0b	Reserved

8.7 DMIVC1RCAP—DMI VC1 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 1C–1Fh
Default Value: 00008001h
Access: RO
Size: 32 bits

Bit	Access	Default Value	Description
31:16	RO	00h	Reserved
15	RO	1b	**Reject Snoop Transactions (REJSNPT):** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
14:8	RO	00h	Reserved
7:0	RO	01h	**Port Arbitration Capability (PAC):** Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

8.8 DMIVC1RCTL1—DMI VC1 Resource Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 20–23h
Default Value: 01000000h
Access: RW, RO
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access	Default Value	Description
31	RW	0b	**Virtual Channel 1 Enable (VC1E):** 0 = Virtual Channel is disabled. 1 = Virtual Channel is enabled.
30:27	RO	0h	Reserved
26:24	RW	001b	**Virtual Channel 1 ID (VC1ID):** This field assigns a VC ID to the VC resource. Assigned value must be non-zero. This field can not be modified when the VC is already enabled.
23:20	RO	0h	Reserved
19:17	RW	000b	**Port Arbitration Select (PAS):** This field configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource.
16:8	RO	000h	Reserved
7:1	RW	00h	**Traffic Class / Virtual Channel 1 Map (TCVC1M):** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. To remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO	0b	**Traffic Class 0 / Virtual Channel 1 Map (TC0VC1M):** Traffic Class 0 is always routed to VC0.

8.9 DMIVC1RSTS—DMI VC1 Resource Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 26–27h
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access	Default Value	Description
15:2	RO	0000h	Reserved
1	RO	1b	**Virtual Channel 1 Negotiation Pending (VC1NP):** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling).
0	RO	0b	Reserved

8.10 DMILCAP—DMI Link Capabilities

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 84–87h
Default Value: 00012C41h
Access: RO, RWO
Size: 32 bits

This register indicates DMI specific capabilities.

Bit	Access	Default Value	Description
31:18	RO	0000h	Reserved
17:15	RWO	010b	**L1 Exit Latency (L1SELAT):** This field indicates the length of time this Port requires to complete the transition from L1 to L0. 010 = 2 µs to less than 4 µs All other encodings are reserved.
14:12	RWO	010b	Reserved
11:10	RO	11b	**Active State Link PM Support (ASLPMS):** L1 entry supported.
9:4	RO	04h	**Max Link Width (MLW):** This field indicates the maximum number of lanes supported for this link. 04h = x4 All other encodings are reserved.
3:0	RO	1h	**Max Link Speed (MLS):** Hardwired to indicate 2.5 Gb/s.

8.11 DMILCTL—DMI Link Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 88–89h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

This register allows control of DMI.

Bit	Access	Default Value	Description
15:8	RO	00h	Reserved
7	RW	0b	**Extended Synch (EXTSYNC):** 0 = Standard Fast Training Sequence (FTS). 1 = Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state.
6:3	RO	0h	Reserved
2	RW	0b	**Far-End Digital Loopback (FEDLB):**
1:0	RW	00b	**Active State Power Management Support (ASPMS):** This field controls the level of active state power management supported on the given link. 00 = Disabled 01 = Reserved 10 = Reserved 11 = L1 Entry Supported

8.12 DMILSTS—DMI Link Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 8A–8Bh
Default Value: 0001h
Access: RO
Size: 16 bits

This register indicates DMI status.

Bit	Access	Default Value	Description
15:4	RO	0s	Reserved
3:0	RO	1h	**Negotiated Speed (NSPD):** This field indicates negotiated link speed. 1h = 2.5 Gb/s All other encodings are reserved.

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9 Functional Description

9.1 Host Interface

The MCH supports the Intel® Core™2 Duo processors, Intel® Core™2 Quad processors, Intel® Core™2 Extreme processors, and Intel® Core™2 Extreme processor QX9770 at 1600 FSB. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. The address signals are double pumped and a new address can be generated every other bus clock. At 200/267/333/400 MHz bus clock the address signals run at 800MT/s. The data is quad pumped and an entire 64B cache line can be transferred in two bus clocks. At 200/266/333/400 MHz bus clock, the data signals run at 800/1066/1333/1600 MT/s for a maximum bandwidth of 6.4/ 8.5/10.6/12.8 GB/s.

9.1.1 FSB IOQ Depth

The Scalable Bus supports up to 12 simultaneous outstanding transactions.

9.1.2 FSB OOQ Depth

The MCH supports only one outstanding deferred transaction on the FSB.

9.1.3 FSB GTL+ Termination

The MCH integrates GTL+ termination resistors on die.

9.1.4 FSB Dynamic Bus Inversion

The MCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the processor. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the MCH. HDINV[3:0]# indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

HDINV[3:0]#	Data Bits
HDINV0#	HD[15:0]#
HDINV1#	HD[31:16]#
HDINV2#	HD[47:32]#
HDINV3#	HD[63:48]#

Whenever the processor or the MCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus, the corresponding HDINV# signal will be asserted, and the data will be inverted prior to being driven on the bus. Whenever the processor or the MCH receives data, it monitors HDINV#[3:0] to determine if the corresponding data segment should be inverted.

Table 15. Host Interface 4X, 2X, and 1X Signal Groups

Signals	Associated Clock or Strobe	Signal Group
ADS#, BNR#, BPRI#, DEFER#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, RS[2:0]#, TRDY#, RESET, BR0#	BCLK	1X
HA[16:3]#, REQ[4:0]#	ADSTB[0]#	2X
HA[35:17]#	ADSTB[1]#	
D[15:0]#, DBI0#	DSTBP0#, DSTBN0#	4X
D[31:16]#, DBI1#	DSTBP1#, DSTBN1#	
D[47:32]#, DBI2#	DSTBP2#, DSTBN2#	
D[63:48]#, DBI3#	DSTBP3#, DSTBN3#	

9.1.5 APIC Cluster Mode Support

APIC Cluster mode support is required for backwards compatibility with existing software, including various OSes.

The MCH supports three types of interrupt re-direction:

- Physical
- Flat-Logical
- Clustered-Logical

9.2 System Memory Controller

The system memory controller supports DDR3 protocols with two independent 64 bit wide channels each accessing one or two DIMMs. It supports a maximum of two un-buffered non-ECC DDR3 DIMMs per channel; thus, allowing up to four device ranks per channel.

9.2.1 System Memory Organization Modes

The system memory controller supports two memory organization modes: Single Channel and Dual Channel.

9.2.1.1 Single Channel Mode

In this mode, all memory cycles are directed to a single channel.

Single channel mode is used when either Channel A or Channel B DIMMs are populated in any order, but not both.

9.2.1.2 Dual Channel Modes

9.2.1.2.1 Dual Channel Symmetric Mode

This mode provides maximum performance on real applications. Addresses are ping-ponged between the channels after each cache line (64 byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are guaranteed to be on opposite channels.

Dual channel symmetric mode is used when both Channel A and Channel B DIMMs are populated in any order with the total amount of memory in each channel being the same, but the DRAM device technology and width may vary from one channel to the other.

Table 16 is a sample dual channel symmetric memory configuration showing the rank organization.

Table 16. Sample System Memory Dual Channel Symmetric Organization Mode

Rank	Channel 0 Population	Cumulative Top Address in Channel 0	Channel 1 Population	Cumulative Top Address in Channel 1
Rank 3	0 MB	2560 MB	0 MB	2560 MB
Rank 2	256 MB	2560 MB	256 MB	2560 MB
Rank 1	512 MB	2048 MB	512 MB	2048 MB
Rank 0	512 MB	1024 MB	512 MB	1024 MB

9.2.1.2.2 Dual Channel Asymmetric Mode with Intel® Flex Memory Mode Enabled

In this addressing mode the lowest DRAM memory is mapped to dual channel operation and the top most DRAM memory is mapped to single channel operation. In this mode the system can run at one zone of dual channel mode and one zone of single channel mode simultaneously across the whole memory array.

This mode is used when Intel® Flex Memory Mode is enabled and both Channel A and Channel B DIMMs are populated in any order with the total amount of memory in each channel being different.

Table 17 is a sample dual channel asymmetric memory configuration showing the rank organization with Intel® Flex Memory Mode Enabled:

Table 17. Sample System Memory Dual Channel Asymmetric Organization Mode with Intel® Flex Memory Mode Enabled

Rank	Channel 0 Population	Cumulative Top Address in Channel 0	Channel 1 Population	Cumulative Top Address in Channel 1
Rank 3	0 MB	2048 MB	0 MB	2304 MB
Rank 2	0 MB	2048 MB	256 MB	2304 MB
Rank 1	512 MB	2048 MB	512 MB	2048 MB
Rank 0	512 MB	1024 MB	512 MB	1024 MB

9.2.1.2.3 Dual Channel Asymmetric Mode with Intel® Flex Memory Mode Disabled

In this addressing mode addresses start in channel 0 and stay there until the end of the highest rank in channel 0, and then addresses continue from the bottom of channel 1 to the top.

This mode is used when Intel® Flex Memory Mode is disabled and both Channel A and Channel B DIMMs are populated in any order with the total amount of memory in each channel being different.

Table 18 is a sample dual channel asymmetric memory configuration showing the rank organization with Intel® Flex Memory Mode Disabled:

Table 18. Sample System Memory Dual Channel Asymmetric Organization Mode with Intel® Flex Memory Mode Disabled

Rank	Channel 0 Population	Cumulative Top Address in Channel 0	Channel 1 Population	Cumulative Top Address in Channel 1
Rank 3	0 MB	1280 MB	0 MB	2304 MB
Rank 2	256 MB	1280 MB	0 MB	2304 MB
Rank 1	512 MB	1024 MB	512 MB	2304 MB
Rank 0	512 MB	512 MB	512 MB	1792 MB

9.2.2 System Memory Technology Supported

The MCH supports the following DDR3 Data Transfer Rates, DIMM Modules, and DRAM Device Technologies:

- DDR3 Data Transfer Rates: 800 (PC3-6400), 1066 (PC3-8500), and 1333 (PC3-10600), and 1600 (PC3-12800)
- DDR3 DIMM Modules:
  - — Raw Card A - Single Sided x8 un-buffered non-ECC
  - — Raw Card B - Double Sided x8 un-buffered non-ECC
  - — Raw Card C - Single Sided x16 un-buffered non-ECC
  - — Raw Card F - Double Sided x16 un-buffered non-ECC
- DDR3 DRAM Device Technology: 512-Mb and 1-Gb

Table 19. Supported DIMM Module Configurations

Memory Type	Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Physical Device Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
DDR3 800, 1066, 1333, and 1600(1,2)	A	512 MB	512Mb	64M X 8	8	1	13/10	8	8K
		1 GB	1Gb	128M X 8	8	1	14/10	8	8K
	B	1 GB	512Mb	64M X 8	16	2	13/10	8	8K
		2 GB	1Gb	128M X 8	16	2	14/10	8	8K
	C	256 MB	512Mb	32M X 16	4	1	12/10	8	8K
		512 MB	1Gb	64M X 16	4	1	13/10	8	8K
	F	512 MB	512Mb	32M X 16	8	2	12/10	8	8K
		1 GB	1Gb	64M X 16	8	2	13/10	8	8K

NOTES:
1. The MCH requires Intel® XMP DDR3-1600 DIMM for 1600 MHz DDR3 speeds.
2. The MCH using Intel® XMP DDR3-1600 DIMMs support only single DIMM single rank memory configurations where DIMM1 is populated and DIMM0 is not populated.

9.2.3 Intel® Extreme Memory Profile (XMP) Support

The Intel® Extreme Memory Profile (XMP) provides a simple and robust high performance DDR3 memory solution for Intel based platforms using the Intel® X48 Express Chipset. Intel co-developed the Extreme Memory Profile (XMP) specification with its memory partners to enable performance tuning of DDR3 memory to beyond standard JEDEC SPD specifications. This benefits the user by enabling both the novice (using built-in profiles) and the advanced users (by allowing manual timing parameter adjustments) to tune the performance of their Intel platforms. This profile based solution enables the Intel® X48 Express Chipset to support non-JEDEC defined solutions (e.g., DDR3-1600 and beyond).

The Intel® X48 Express Chipset with Intel® Extreme Memory Profile (XMP) DIMMs enable new extreme levels of memory performance.

9.3 PCI Express*

See Section 1.3 for a list of PCI Express features, and the PCI Express specification for further details.

This MCH is part of a PCI Express root complex. This means it connects a host processor/memory subsystem to a PCI Express hierarchy. The control registers for this functionality are located in Device 1 and Device 6 configuration space and three Root Complex Register Blocks (RCRBs). The DMI RCRB contains registers for control of the Intel ICH9 attach ports.

9.3.1 PCI Express* Architecture

The PCI Express architecture is specified in layers. Compatibility with the PCI addressing model (a load-store architecture with a flat address space) is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial speed of 2.5 GHz results in 5 Gb/s each direction which provides a 500 MB/s communications channel in each direction (1000 MB/s total).

9.3.1.1 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

9.3.1.2 Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

9.3.1.3 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry.

9.4 Power Management

Power Management Feature List:

- ACPI 1.0b support
- ACPI S0, S1, S3 (Cold), S5, C0, and C1 states
- Enhanced power management state transitions for increasing time processor spends in low power states
- PCI Express Link States: L0, L2/L3 Ready, L3

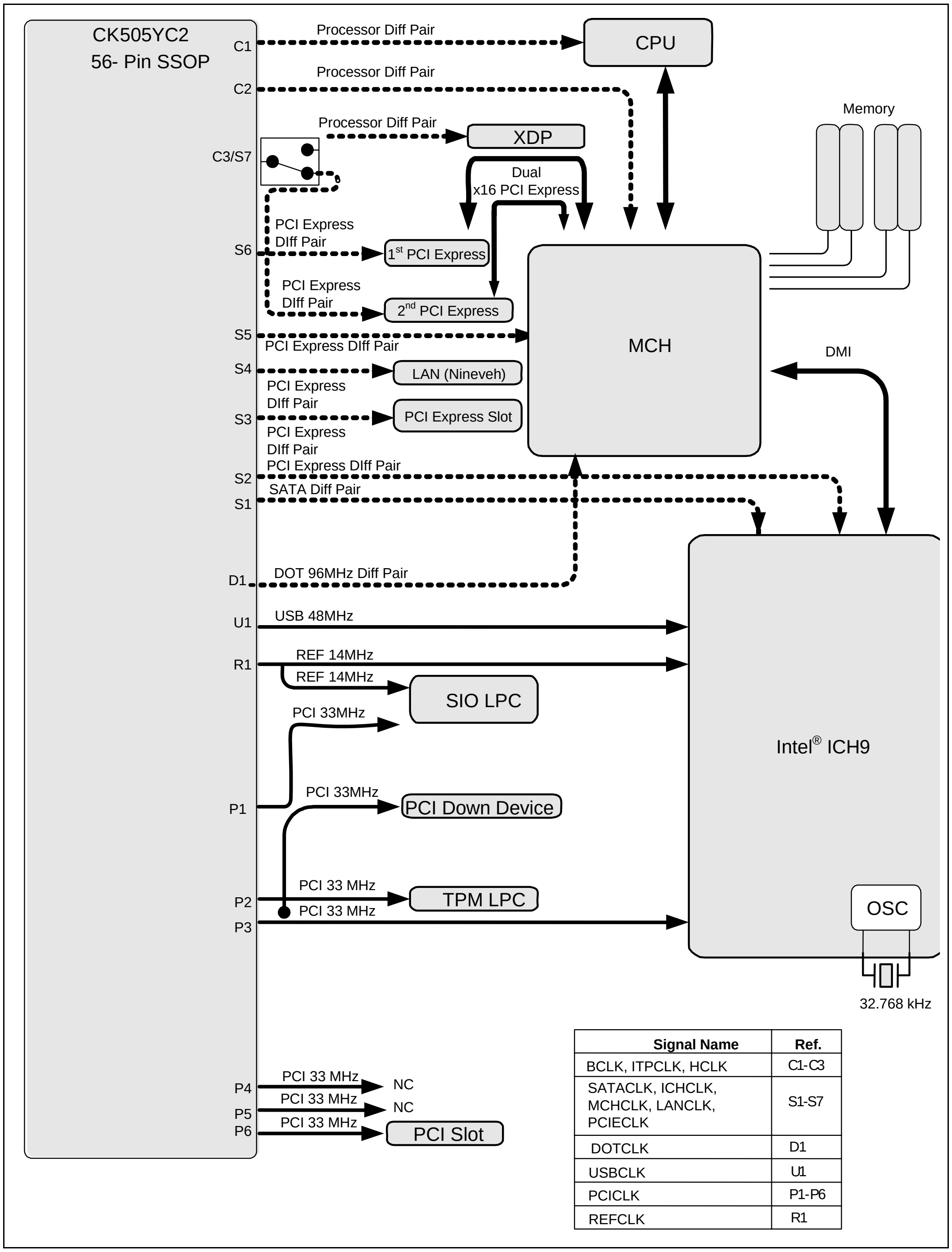
9.5 Clocking

The MCH has a total of 3 PLLs providing many times that many internal clocks. The PLLs are:

- Host PLL – Generates the main core clocks in the host clock domain. Can also be used to generate memory core clocks. Uses the Host clock (H_CLKIN) as a reference.
- Memory I/O PLL - Optionally generates low jitter clocks for memory I/O interface, as opposed to from Host PLL. Uses the Host FSB differential clock (HPL_CLKINP/ HPL_CLKINN) as a reference. Low jitter clock source from memory I/O PLL is required for DDR667 and higher frequencies.
- PCI Express PLL – Generates all PCI Express related clocks, including the Direct Media that connect to the ICH. This PLL uses the 100 MHz clock (EXP_CLKNP/ EXP2_CLKNP) as a reference.

CK505YC2 is the clocking chip required for the platform.

Figure 9. Intel® X48 Chipset Clocking Diagram



Signal Name	Ref.
BCLK, ITPCLK, HCLK	C1-C3
SATACLK, ICHCLK, MCHCLK, LANCLK, PCIECLK	S1-S7
DOTCLK	D1
USBCLK	U1
PCICLK	P1-P6
REFCLK	R1

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10 Electrical Characteristics

This chapter contains the DC for the Intel® X48 Express Chipset MCH.

10.1 Absolute Minimum and Maximum Ratings

Table 20 specifies the MCH absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time its reliability will be severely degraded or not function when returned to conditions within the functional operating condition limits.

Although the MCH contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 20. Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
MCH Core					
VCC	1.25 V Core Supply Voltage with respect to VSS	-0.3	1.375	V	
Host Interface (800/1066/1333/1600 MHz)					
VTT_FSB	System Bus Input Voltage with respect to VSS	-0.3	1.32	V	
VCCA_HPLL	1.25 V Host PLL Analog Supply Voltage with respect to VSS	-0.3	1.375	V	
System Memory Interface (DDR3 800/1066/1333/1600 MHz)					
VCC_DDR	1.5 V / 1.9 V DDR3 System Memory Supply Voltage with respect to VSS	-0.3	4.0	V	1
VCC_CKDDR	1.5 V / 1.9 V DDR3 Clock System Memory Supply Voltage with respect to VSS	-0.3	4.0	V	1
VCCA_MPLL	1.25 V System Memory PLL Analog Supply Voltage with respect to VSS	-0.3	1.375	V	

Table 20. Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
PCI Express* / DMI Interface					
VCC_EXP	1.25 V PCI Express* and DMI Supply Voltage with respect to VSS	-0.3	1.375	V	
VCCA_EXP	3.3 V PCI Express* Analog Supply Voltage with respect to VSS	-0.3	3.63	V	
VCCAPLL_EXP	1.25 V Primary PCI Express* PLL Analog Supply Voltage with respect to VSS	-0.3	1.375	V	
VCCAPLL_EXP2	1.25 V Secondary PCI Express* PLL Analog Supply Voltage with respect to VSS	-0.3	1.375	V	
CMOS Interface					
VCC3_3	3.3 V CMOS Supply Voltage with respect to VSS	-0.3	3.63	V	

NOTES:
1. The 1.9 V System Memory Voltage is only for DDR3-1600 XMP support. For DDR3-800/1066/1333 support, the System Memory Voltage must be 1.5 V.

10.2 Current Consumption

Table 21 shows the current consumption for the MCH in the Advanced Configuration and Power Interface (ACPI) S0 state. I_{CC} max values are determined on a per-interface basis, at the highest frequencies for each interface. Sustained current values or Max current values can not occur simultaneously on all interfaces. Sustained Values are *measured* sustained RMS maximum current consumption and includes leakage estimates. The measurements are made with fast silicon at 96 °C T_{CASE} temperature, at the Max voltage listed in Table 23. The Max values are maximum theoretical pre-silicon calculated values. In some cases, the Sustained measured values have exceeded the Max theoretical values.

Table 21. Current Consumption in S0

Symbol	Parameter	Signal Names	Sustained	Max	Unit	Notes
I_{VCC}	1.25 V Core Supply Current (Discrete Graphics)	VCC	7.49	8.99	A	1,2
$I_{VCC\_DDR\_1.5}$	DDR3 System Memory Interface (1.5 V) Supply Current	VCC_DDR	1.53	1.61	A	1, 2, 3
$I_{VCC\_CKDDR\_1.5}$	DDR3 System Memory Clock Interface (1.5 V) Supply Current	VCC_CKDDR	334	367	mA	
$I_{VCC\_DDR\_1.9}$	DDR3 System Memory Interface (1.9 V) Supply Current	VCC_DDR	2.181	2.285	A	1, 2, 3
$I_{VCC\_CKDDR\_1.9}$	DDR3 System Memory Clock Interface (1.9 V) Supply Current	VCC_CKDDR	506.793	557.473	mA	
I_{VCC_EXP}	1.25 V PCI Express* and DMI Supply Current	VCC_EXP	5.12	6.65	A	2
I_{VTT_FSB}	System Bus Supply Current	VTT_FSB	464	696	mA	1
I_{VCCA_EXP}	3.3 V PCI Express* and DMI Analog Supply Current	VCCA_EXP	167	175	mA	

Table 21. Current Consumption in S0

Symbol	Parameter	Signal Names	Sustained	Max	Unit	Notes
IVCC3_3	3.3 V CMOS Supply Current	VCC3_3	0.5	16	mA	
$I_{VCCAPLL\_EXP}$	1.25 V PCI Express* and DMI PLL Analog Supply Current	VCCAPLL_EXP	48	53	mA	
I_{VCCA_HPLL}	1.25 V Host PLL Supply Current	VCCA_HPLL	21	32	mA	
I_{VCCA_MPLL}	1.25 V System Memory PLL Analog Supply Current	VCCA_MPLL	117	175	mA	

NOTES:
1. Measurements are for current coming through chipset's supply pins.
2. Rail includes DLLs (and FSB sense amps on V_{CC}).
3. Sustained Measurements are combined because one voltage regulator on the platform supplies both rails on the MCH.

10.3 Signal Groups

The signal description includes the type of buffer used for the particular signal:

Type	Description
PCI Express*	PCI Express interface signals. These signals are compatible with PCI Express 2.0 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2 Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
DMI	Direct Media Interface signals. These signals are compatible with PCI Express 1.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2 Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
GTL+	Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details.
HCSL	Host Clock Signal Level buffers. Current mode differential pair. Differential typical swing = (|D+ - D-|) * 2 = 1.4 V. Single ended input tolerant from -0.35V to 1.2 V. Typical crossing voltage 0.35 V.
SSTL-1.5	Stub Series Termination Logic. These are 1.5 V output capable buffers. 1.5 V tolerant.
CMOS	CMOS buffers
Analog	Analog reference or output. May be used as a threshold voltage or for buffer compensation.

Table 22. Signal Groups (Sheet 1 of 2)

Signal Type	Signals
Host Interface Signal Groups	
GTL+ Input/Outputs	FSB_ADSB, FSB_BNRB, FSB_DBSYB, FSB_DINVB_3:0, FSB_DRDYB, FSB_AB_35:3, FSB_ADSTBB_1:0, FSB_DB_63:0, FSB_DSTBPB_3:0, FSB_DSTBNB_3:0, FSB_HITB, FSB_HITMB, FSB_REQB_4:0
GTL+ Common Clock Outputs	FSB_BPRIB, FSB_BREQ0B, FSB_CPURSTB, FSB_DEFERB, FSB_TRDYB, FSB_RSB_2:0
Analog Host I/F Ref & Comp. Signals	FSB_RCOMP, FSB_SCOMP, FSB_SCOMPB, FSB_SWING, FSB_DVREF, FSB_ACCVREF
GTL+ Input	FSB_LOCKB, BSEL2:0
PCI Express* Graphics Interface Signal Groups	
PCI Express* Input	**PCI Express* Interface:** PEG_RXN_15:0, PEG_RXP_15:0
PCI Express* Output	**PCI Express* Interface:** PEG_TXN_15:0, PEG_TXP_15:0
Analog PCI Express* Compensation Signals	EXP_COMPO, EXP_COMPI
Direct Media Interface Signal Groups	
DMI Input	DMI_RXP_3:0, DMI_RXN_3:0
DMI Output	DMI_TXP_3:0, DMI_TXN_3:0
System Memory Interface Signal Groups	
SSTL-1.5 Input/ Output	DDR_A_DQ_63:0, DDR_A_DQS_7:0, DDR_A_DQSB_7:0 DDR_B_DQ_63:0, DDR_B_DQS_7:0, DDR_B_DQSB_7:0
SSTL-1.5 Output	DDR_A_CK_5:0, DDR_A_CKB_5:0, DDR_A_CSB_3:2, DDR3_A_CSB_1, DDR_A_CSB_0, DDR_A_CKE_3:0, DDR_A_ODT_3:0, DDR_A_MA_14:1, DDR3_A_MA_0, DDR_A_BS_2:0, DDR_A_RASB, DDR_A_CASB, DDR3_A_WEB, DDR_A_DM_7:0 DDR_B_CK_5:0, DDR_B_CKB_5:0, DDR_B_CSB_3:0, DDR_B_CKE_3:0, DDR_B_ODT_2:0, DDR3_B_ODT_3, DDR_B_MA_14:0, DDR_B_BS_2:0, DDR_B_RASB, DDR_B_CASB, DDR_B_WEB, DDR_B_DM_7:0 DDR3_DRAMRST
CMOS Input	DDR3_DRAM_PWROK
Reference and Comp. Voltages	DDR_RCOMPXPD, DDR_RCOMPXPU, DDR_RCOMPYPD, DDR_RCOMPYPU, DDR_VREF
Clocks	
HCSL	HPL_CLKINP, HPL_CLKINN, EXP_CLKINP, EXP_CLKINN, DPL_REFCLKINN, DPL_REFCLKINP
Reset, and Miscellaneous Signal Groups	
CMOS Input	EXP_SLR, PWROK, RSTINB
CMOS Output	ICH_SYNCB

Table 22. Signal Groups (Sheet 2 of 2)

Signal Type	Signals
I/O Buffer Supply Voltages	
System Bus Input Supply Voltage	VTT_FSB
1.25 V PCI Express* Supply Voltages	VCC_EXP
3.3 V PCI Express* Analog Supply Voltage	VCCA_EXP
1.5 V / 1.9 V DDR3 System Memory Supply Voltage	VCC_DDR
1.5 V / 1.9 V DDR3 System Memory Clock Supply Voltage	VCC_CKDDR
1.25 V MCH Core Supply Voltage	VCC
3.3 V CMOS Supply Voltage	VCC3_3
PLL Analog Supply Voltages	VCCA_HPLL, VCCAPLL_EXP, VCCA_MPLL

10.4 Buffer Supply and DC Characteristics

10.4.1 I/O Buffer Supply Voltages

The I/O buffer supply voltage is measured at the MCH package pins. The tolerances shown in Table 23 are inclusive of all noise from DC up to 20 MHz. In the lab, the voltage rails should be measured with a bandwidth limited oscilloscope with a roll off of 3 dB/decade above 20 MHz under all operating conditions.

Table 23 indicates which supplies are connected directly to a voltage regulator or to a filtered voltage rail. For voltages that are connected to a filter, they should be measured at the *input* of the filter.

If the recommended platform decoupling guidelines cannot be met, the system designer will have to make tradeoffs between the voltage regulator output DC tolerance and the decoupling performance of the capacitor network to stay within the voltage tolerances listed in Table 23.

Table 23. I/O Buffer Supply Voltage

Symbol	Parameter	Min	Nom	Max	Unit	Notes
VCC_DDR	DDR3 1.9 V I/O Supply Voltage	1.825	1.9	1.975	V	
VCC_DDR	DDR3 1.5 V I/O Supply Voltage	1.425	1.5	1.575	V	
VCC_CKDDR	DDR3 1.9 V Clock Supply Voltage	1.825	1.9	1.975	V	1
VCC_CKDDR	DDR3 1.5 V Clock Supply Voltage	1.425	1.5	1.575	V	1
VCC_EXP	PCI-Express* Supply Voltage	1.188	1.25	1.313	V	
VCCA_EXP	PCI-Express* Analog Supply Voltage	3.135	3.3	3.465	V	1
VTT_FSB	1.2 V System Bus Input Supply Voltage	1.14	1.2	1.26	V	2
	1.1 V System Bus Input Supply Voltage	1.045	1.1	1.155	V	
VCC	MCH Core Supply Voltage	1.188	1.25	1.313	V	
VCC3_3	CMOS Supply Voltage	3.135	3.3	3.465	V	
VCCA_HPLL, VCCAPLL_EXP, VCCA_MPLL	Various PLL Analog Supply Voltages	1.188	1.25	1.313	V	1

NOTES:
1. These rails are filtered from other voltage rails on the platform and should be measured at the input of the filter.
2. MCH supports both V_{TT} = 1.2 V nominal and V_{TT} = 1.1 V nominal depending on the identified processor.

10.4.2 General DC Characteristics

Platform Reference Voltages at the top of Table 24 are specified at DC only. V_{REF} measurements should be made with respect to the supply voltage.

Table 24. DC Characteristics (Sheet 1 of 3)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
Reference Voltages						
FSB_DVREF FSB_ACCVREF	Host Data, Address, and Common Clock Signal Reference Voltages	0.666 x VTT_FSB –2%	0.666 x VTT_FSB	0.666 x VTT_FSB +2%	V	
FSB_SWING	Host Compensation Reference Voltage	0.25 x VTT_FSB –2%	0.25 x VTT_FSB	0.25 x VTT_FSB +2%	V	
DDR_VREF	DDR3 Reference Voltage	0.49 x VCC_DDR	0.50 x VCC_DDR	0.51 x VCC_DDR	V	
Host Interface						
V_{IL_H}	Host GTL+ Input Low Voltage	-0.10	0	(0.666 x VTT_FSB) – 0.1	V	
V_{IH_H}	Host GTL+ Input High Voltage	(0.666 x VTT_FSB) + 0.1	VTT_FSB	VTT_FSB + 0.1	V	
V_{OL_H}	Host GTL+ Output Low Voltage	—	—	(0.25 x VTT_FSB) + 0.1	V	
V_{OH_H}	Host GTL+ Output High Voltage	VTT_FSB – 0.1	—	VTT_FSB	V	
I_{OL_H}	Host GTL+ Output Low Current	—	—	VTT_FSBmax * (1–0.25) / Rttmin	mA	Rtt_{min} = 47.5 Ω
I_{LEAK_H}	Host GTL+ Input Leakage Current	—	—	45	µA	V_{OL}< Vpad< Vtt_FSB
C_{PAD}	Host GTL+ Input Capacitance	2.0	—	2.5	pF	
C_{PCKG}	Host GTL+ Input Capacitance (common clock)	0.90	—	2.5	pF	
DDR3 System Memory Interface						
$V_{IL(DC)}$	DDR3 Input Low Voltage	—	—	DDR_VREF – 0.100	V	
$V_{IH(DC)}$	DDR3 Input High Voltage	DDR_VREF + 0.100	—	—	V	
$V_{IL(AC)}$	DDR3 Input Low Voltage	—	—	DDR_VREF – 0.175	V	
$V_{IH(AC)}$	DDR3 Input High Voltage	DDR_VREF + 0.175	—	—	V	
V_{OL}	DDR3 Output Low Voltage	—	—	0.2 * VCC_DDR	V	1

Table 24. DC Characteristics (Sheet 2 of 3)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_{OH}	DDR3 Output High Voltage	0.8 * VCC_DDR	—	—	V	1
I_{Leak}	Input Leakage Current	—	—	±20	µA	4
I_{Leak}	Input Leakage Current	—	—	±550	µA	5
$C_{I/O}$	DQ/DQS/DQSB DDR3 Input/Output Pin Capacitance	1.0	—	4.0	pF	
1.25 V PCI Express* Interface 2.0						
$V_{TX\text{-}DIFF\ P\text{-}P}$	Differential Peak to Peak Output Voltage	0.800	—	1.2	V	2
$V_{TX\_CM\text{-}ACp}$	AC Peak Common Mode Output Voltage	—	—	20	mV	
$Z_{TX\text{-}DIFF\text{-}DC}$	DC Differential TX Impedance	80	100	120		
$V_{RX\text{-}DIFF\ p\text{-}p}$	Differential Peak to Peak Input Voltage	0.175	—	1.2	V	3
$V_{RX\_CM\text{-}ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	
Input Clocks						
V_{IL}	Input Low Voltage	-0.150	0	N/A	V	
V_{IH}	Input High Voltage	0.660	0.710	0.850	V	
$V_{CROSS(ABS)}$	Absolute Crossing Voltage	0.300	N/A	0.550	V	6,7,8
$V_{CROSS(REL)}$	Range of Crossing Points	N/A	N/A	0.140	V	
C_{IN}	Input Capacitance	1	—	3	pF	
PWROK, RSTIN#						
V_{IL}	Input Low Voltage	—	—	0.3	V	
V_{IH}	Input High Voltage	2.7	—	—	V	
I_{LEAK}	Input Leakage Current	—	—	±1	mA	
C_{IN}	Input Capacitance	—	—	6.0	pF	
ICH_SYNCB						
I_{OL}	Output Low Current (CMOS Outputs)	—	—	2.0	mA	@V_{OL_HI} max
I_{OH}	Output High Current (CMOS Outputs)	-2.0	—	—	mA	@V_{OH_HI} min
V_{OL}	Output Low Voltage (CMOS Outputs)	—	—	0.33	V	

Table 24. DC Characteristics (Sheet 3 of 3)

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_{OH}	Output High Voltage (CMOS Outputs)	2.97	—	—	V	
EXP_SLR, EXP_EN						
V_{IL}	Input Low Voltage	-0.10	0	(0.63 x VTT) – 0.1	V	
V_{IH}	Input High Voltage	(0.63 x VTT)+0.1	VTT	VTT +0.1	V	
I_{LEAK}	Input Leakage Current	—	—	20	µA	V_{OL} < Vpad < V_{TT}
C_{IN}	Input Capacitance	2	—	2.5	pF	

NOTES:

1. Determined with 2x MCH Buffer Strength Settings into a 50 Ω to 0.5xVCC_DDR test load.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of PCI Express* specification and measured over any 250 consecutive TX UIs.
3. Specified at the measurement point over any 250 consecutive UIs. The test load shown in Receiver compliance eye diagram of PCI Express* spec should be used as the RX device when taking measurements.
4. Applies to pin to VCC or VSS leakage current for the DDR_A_DQ_63:0 and DDR_B_DQ_63:0 signals.
5. Applies to pin to pin leakage current between DDR_A_DQS_7:0, DDR_A_DQSB_7:0, DDR_B_DQS_7:0, and DDR_B_DQSB_7:0 signals.
6. Crossing voltage defined as instantaneous voltage when rising edge of BCLK0 equals falling edge of BCLK1.
7. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
8. The crossing point must meet the absolute and relative crossing point specifications simultaneously. Refer to the appropriate processor datasheet for further information.

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11 Ballout and Package Information

This chapter provides the ballout and package dimensions for the MCH.

11.1 Ballout

Figure 10, Figure 11, and Figure 12 provide the MCH ballout as viewed from the top side of the package. Table 25 provides a ballout list arranged alphabetically by signal name. Table 26 provides a ballout list arranged numerically by ball number.

Note: Notes for Figure 10, Figure 11, Figure 12, Table 25 and Table 26.

1. Balls that are listed as RSVD are reserved.
2. Some balls marked as reserved (RSVD) are used in XOR testing. See Chapter 12 for details.
3. Balls that are listed as NC are No Connects.

Figure 10. MCH Ballout Diagram (Top View Left – Columns 45–31)

	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	
BE	TEST0	VCC_CKDDR	VCC_CKDDR			VCC_DDR		VSS		VCC_DDR		VSS		VCC_DDR		BE
BD	NC	VCC_CKDDR	VCC_CKDDR	DDR_A_CSB_1			DDR_A_WEB		DDR_A_MA_10		DDR3_A_MA0		DDR_B_ODT_0		DDR_B_RASB	BD
BC	VCC_CKDDR	VCC_CKDDR	VSS	DDR_RCOMPYPD		DDR3_A_WEB		VCC_DDR	DDR_A_BS_0	DDR_A_MA_0		VCC_DDR		DDR_B_CSB_2		BC
BB		DDR3_A_CSB1	DDR_A_ODT_0	DDR_RCOMPYPU	DDR_A_CASB		DDR_A_CSB_2	DDR_A_RASB		DDR_A_BS_1	DDR_B_CSB_1	DDR_B_ODT_1	DDR_B_ODT_2	DDR_B_CASB	DDR_A_MA_1	BB
BA				DDR_A_MA_13	DDR_A_ODT_2	DDR_A_CSB_0			DDR3_B_ODT3		DDR_B_CSB_3		DDR_B_MA_13		DDR_B_CSB_0	BA
AY	VCC_DDR		DDR_A_CSB_3		DDR_A_ODT_1	DDR_B_DM_4	DDR_B_DQ_32	DDR_B_DQ_36		VSS	DDR_B_ODT_3	DDR_B_CKB_5	VSS		DDR_B_WEB	AY
AW		DDR_A_ODT_3		DDR_A_DQ_36		VSS	DDR_B_DQS_4	DDR_B_DQ_33		DDR_B_DQ_37	VSS	DDR_B_CK_5	DDR_B_CKB_2		VSS	AW
AV	VSS		VSS	DDR_A_DQ_32		DDR_B_DQ_39	DDR_B_DQ_38	DDR_B_DQSB_4		DDR_B_DQ_44	DDR_A_CKB_2	VSS	DDR_B_CK_2		DDR_A_CK_3	AV
AU		DDR_A_DM_4	DDR_A_DQ_33		DDR_A_DQ_37											AU
AT	VSS		DDR_A_DQS_4	DDR_A_DQSB_4		DDR_B_DQ_35	VSS	DDR_B_DQ_34		DDR_A_CKB_5	DDR_A_CK_5	DDR_A_CK_2	DDR_A_CK_0		DDR_A_CKB_3	AT
AR		DDR_A_DQ_34		DDR_A_DQ_35	DDR_A_DQ_38	DDR_A_DQ_39	VSS	VSS		DDR_B_DQ_40	VSS	DDR_B_DQ_45	DDR_A_CKB_0		DDR_B_CK_3	AR
AP	DDR_A_DQ_45		VSS	DDR_A_DQ_44		DDR_B_DQSB_5	DDR_B_DQS_5	VSS		DDR_B_DQ_41	DDR_B_DQ_42	RSVD	VSS		DDR_B_CKB_3	AP
AN		DDR_A_DM_5		DDR_A_DQ_41	DDR_A_DQ_40	DDR_B_DQ_47	DDR_B_DQ_46	VSS		DDR_B_DM_5	DDR_A_CB_1	VSS	DDR_B_DQ_43		RSVD	AN
AM	VSS		DDR_A_DQS_5	DDR_A_DQSB_5										RSVD		AM
AL		DDR_A_DQ_42		DDR_A_DQ_43	DDR_A_DQ_47	DDR_A_DQ_46	VSS	DDR_A_DQS_8		DDR_A_DQSB_8	VSS	DDR_A_CB_5	DDR_A_CB_0			AL
AK	DDR_B_CB_0		VSS	DDR_B_CB_5		VSS	DDR_A_CB_7	DDR_A_CB_2		VSS	DDR_A_CB_3	DDR_A_CB_6	DDR_A_CB_4	VSS	VCC_CL	AK
AJ		DDR_B_CB_1		DDR_B_CB_4	VSS											AJ
AH	VSS		DDR_B_DQS_8	DDR_B_DQSB_8		VSS	VSS	VSS		DDR_B_DQ_53	VSS	DDR_B_DQ_48	DDR_B_DQ_52	VSS	VCC_CL	AH
AG		DDR_B_CB_7		DDR_B_CB_2	DDR_B_CB_6	DDR_B_CB_3	DDR_B_DQS_6	DDR_B_DQSB_6		VSS	DDR_B_DM_6	VSS	DDR_B_DQ_49	RSVD	VCC_CL	AG
AF	DDR_A_DQ_53		VSS	DDR_A_DQ_52												AF
AE		DDR_A_DM_6		DDR_A_DQ_49	DDR_A_DQ_48	DDR_B_DQ_54	DDR_B_DQ_50	DDR_B_DQ_51		VSS	DDR_B_DQ_60	DDR_B_DQ_61	DDR_B_DQ_55	VSS	VCC_CL	AE
AD	VSS		DDR_A_DQS_6	DDR_A_DQSB_6		DDR_A_DQ_54	DDR_B_DQ_56	VSS		DDR_B_DQ_57	DDR_B_DM_7	VSS	DDR_B_DQSB_7	RSVD	VCC_CL	AD
AC	DDR_A_DQ_51		VSS	DDR_A_DQ_50		DDR_A_DQ_60	DDR_A_DQ_55	VSS		DDR_B_DQ_62	VSS	DDR_B_DQ_63	DDR_B_DQS_7	VSS	VCC_CL	AC
AB	VSS		DDR_A_DQ_57	DDR_A_DQ_56		DDR_A_DM_7	DDR_A_DQ_61	DDR_B_DQ_59		VSS	FSB_AB_34	FSB_AB_29	VSS	DDR_B_DQ_58	VCC_CL	AB
AA		DDR_A_DQSB_7		DDR_A_DQS_7	DDR_A_DQ_62	FSB_AB_33	VSS	FSB_AB_35		VSS	FSB_AB_32	VSS	FSB_AB_31	VSS	VCC_CL	AA
Y	DDR_A_DQ_63		VSS	DDR_A_DQ_58												Y
W		FSB_BREQ0B		DDR_A_DQ_59	FSB_RSB_1	FSB_TRDYB	VSS	FSB_AB_22		FSB_AB_30	VSS	FSB_AB_25	FSB_AB_27	RSVD	VSS_W31	W
V	VSS		FSB_AB_28	FSB_HITMB		VSS	FSB_AB_24	FSB_AB_23		VSS	FSB_AB_26	FSB_ADSTBB_1	VSS	RSVD	VCC_CL	V
U		FSB_ADSB		FSB_BNRB	FSB_DRDYB											U
T	FSB_LOCKB		VSS	FSB_DBSYB		FSB_AB_17	FSB_DEFERB	FSB_AB_20		FSB_AB_18	VSS	FSB_AB_19	RSVD	VSS	VCCAUX	T
R		FSB_RSB_0		FSB_HITB	FSB_RSB_2	VSS	FSB_AB_14	VSS		FSB_AB_10	FSB_AB_16	VSS	RSVD			R
P	VSS		FSB_AB_21	FSB_DB_0										VSS		P
N		FSB_DB_2		FSB_DB_4	FSB_DB_1	FSB_AB_9	FSB_AB_11	FSB_AB_13		FSB_AB_8	VSS	FSB_AB_12	FSB_DB_28		FSB_DB_30	N
M	FSB_DB_5		VSS	FSB_DB_3		FSB_ADSTBB_0	VSS	FSB_AB_4		FSB_AB_5	VSS	VSS	VSS		FSB_DB_31	M
L		FSB_DB_6		FSB_DB_7	FSB_DINVB_0	FSB_AB_7	FSB_REQB_2	VSS		FSB_DB_19	VSS	FSB_DB_27	FSB_DB_29		VSS	L
K	VSS		FSB_DSTBNB_0	FSB_AB_15		VSS	VSS	FSB_AB_6		FSB_REQB_3	FSB_DB_21	FSB_DB_24	VSS		FSB_DB_33	K
J		FSB_DSTBPB_0	FSB_DB_8		FSB_DB_10											J
H	FSB_DB_12		VSS	FSB_DB_9		VSS	FSB_REQB_4	FSB_BPRIB		VSS	VSS	FSB_DSTBPB_1	FSB_DB_25		FSB_DB_34	H
G		FSB_DB_13		FSB_DB_11		FSB_REQB_1	VSS	FSB_DB_20		FSB_DB_22	FSB_DB_23	FSB_DSTBNB_1	VSS		VSS	G
F	VSS		FSB_AB_3		FSB_DB_14	VSS	FSB_DB_17	FSB_DB_16		VSS	FSB_DB_48	VSS	FSB_DB_26		FSB_DB_32	F
E				FSB_DB_15	FSB_DB_50	FSB_DINVB_1			FSB_DB_61		FSB_DB_63		VTT_FSB		VTT_FSB	E
D		FSB_DB_52	FSB_DB_53	VSS	FSB_DSTBNB_3		FSB_DB_57	FSB_DB_54		FSB_DB_59	FSB_CPURSTB	VSS	VTT_FSB	VTT_FSB	VTT_FSB	D
C	VSS	FSB_REQB_0	VSS	FSB_DB_51		FSB_DSTBPB_3		VSS	FSB_DB_60	FSB_DB_58		VSS		VTT_FSB		C
B	NC	VSS	FSB_DB_18	FSB_DB_55			FSB_DB_56		FSB_DINVB_3		FSB_DB_62		VTT_FSB		VTT_FSB	B
A	TEST3	NC	VSS			VSS		FSB_DB_49		VSS		VSS		VTT_FSB		A
	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	

Figure 11. MCH Ballout Diagram (Top View Left – Columns 30–16)

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
BE	VSS		VCC_DDR		VSS		VCC_DDR	VSS	VCC_DDR		DDR_B_MA_8		VSS		DDR_A_DQ_19	BE
BD		DDR_A_MA_6		DDR_A_MA_11		DDR_A_CKE_0				DDR_B_MA_4		DDR_B_CKE_1		DDR_B_CKE_0		BD
BC	VCC_DDR		DDR_A_MA_8		VCC_DDR		DDR_A_CKE_3	VCC_DDR	DDR_B_MA_1		VCC_DDR		DDR_B_MA_14		VSS	BC
BB	DDR_A_MA_2	DDR_A_MA_3	DDR_A_MA_5	DDR_A_MA_12	DDR_A_BS_2	DDR_A_CKE_2	DDR_B_BS_0	DDR3_DRAMRSTB	DDR_B_MA_2	DDR_B_MA_5	DDR_B_MA_6	DDR_B_MA_9	DDR_B_BS_2	DDR_B_CKE_2	DDR_A_DQ_18	BB
BA		DDR_A_MA_4		DDR_A_MA_9		DDR_A_MA_14				DDR_B_MA_3		DDR_B_MA_11		DDR_B_CKE_3		BA
AY	DDR_B_CK_4		DDR_B_CKB_4	DDR_A_MA_7		DDR_B_DM_3	DDR_A_CKE_1	VCC_DDR	DDR_B_MA_0	DDR_A_DQ_25		DDR_B_MA_7	DDR_B_MA_12		DDR_B_DQ_16	AY
AW	DDR_B_CK_0		VSS	VSS		DDR_B_DQ_24	DDR_B_MA_10	DDR_B_BS_1	DDR_A_DQ_31	VSS		DDR_A_DQ_29	VSS		DDR_B_DM_2	AW
AV	DDR_B_CKB_0		VSS	DDR_B_DQ_27		DDR_B_DQ_25	VSS	VSS	VSS	DDR_A_DQSB_3		DDR_A_DQ_28	VSS		DDR_B_DQ_17	AV
AU																AU
AT	VSS		VSS	DDR_B_DQ_26		DDR_B_DQ_30	VSS	VSS	DDR_A_DQ_27	DDR_A_DQS_3		DDR_B_DQ_19	DDR_B_DQ_22		VSS	AT
AR	VSS		DDR_B_CK_1	VSS		DDR_B_DQS_3	DDR_B_DQSB_3	VSS	VSS	VSS		VSS	DDR_B_DQ_23		DDR_B_DQ_21	AR
AP	VSS		DDR_B_CKB_1	DDR_B_DQ_31		VSS	DDR_B_DQ_29	VSS	VSS	DDR_A_DM_3		DDR_B_DQ_18	VSS		DDR_B_DQSB_2	AP
AN	RSVD		DDR_A_CK_1	DDR_A_CK_4		RSVD	DDR_B_DQ_28	VSS	DDR_A_DQ_26	DDR_A_DQ_30		DDR_A_DQ_24	DDR_B_DQS_2		DDR_B_DQ_20	AN
AM	VCC_CL		DDR_A_CKB_1	DDR_A_CKB_4		RSVD	VSS	VCC_CL	VCC_CL	VSS		PWROK	RSTINB		VSS	AM
AL	VCC_CL		RSVD	VCC_CL		VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	AL
AK																AK
AJ		VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL		AJ
AH		VCC_CL	RSVD	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC	VCC		AH
AG		VCC_CL	RSVD	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC		AG
AF		VCC_CL	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC		AF
AE		VCC_CL	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC		AE
AD		VCC_CL	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC		AD
AC		VCC_CL	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC		AC
AB		VCC_CL	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC		AB
AA		VCC_CL	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC		AA
Y		VCC_CL	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC		Y
W		VCC_CL	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC		W
V		VCC_CL	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC		V
U		VCCAUX	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		U
T																T
R	VCCAUX		VCCAUX	VCCAUX		VCCAUX	VCCAUX	VCCAUX	RSVD	VSS		RSVD	VCC		VCC	R
P	HPL_CLKINN		HPL_CLKINP	VSS		VSS	VSS	VSS	VSS	RSVD		RSVD_P19	VSS		ICH_SYNCB	P
N	FSB_DB_37		FSB_DINVB_2	VSS		FSB_DSTBPB_2	FSB_DB_42	VSS	VSS	RSVD		VSS	RSVD		VSS	N
M	FSB_DB_35		VSS	VTT_FSB		FSB_DSTBNB_2	VSS	VSS	BSEL0	ALLZTEST		RSVD_M19	VSS		RSVD	M
L	FSB_DB_36		FSB_DB_41	VTT_FSB		FSB_DB_43	FSB_DB_44	VSS	XORTEST	VSS		RSVD	EXP_EN		VCC3_3_L16	L
K	VSS		FSB_DB_40	VTT_FSB		VTT_FSB	FSB_DB_46	VSS	RSVD	RSVD		EXP_SLR	VSS		RSVD_K16	K
J																J
H	FSB_DB_39		VTT_FSB	VTT_FSB		VTT_FSB	FSB_DB_45	VSS	VSS	RSVD		VSS	VSS		RSVD_H16	H
G	FSB_DB_38		VTT_FSB	VTT_FSB		VTT_FSB	FSB_DB_47	VSS	RSVD	TCEN		MTYPE	VSS		VCC3_3_G16	G
F	VTT_FSB		VTT_FSB	VTT_FSB		VTT_FSB	VSS	VSS	VSS_F22	BSEL1		RSVD	BSEL2		VSS	F
E		VTT_FSB		FSB_DVREF		VCC_E25				VSS		VSS		PEG_TXN_0		E
D	VTT_FSB	VSS	FSB_SCOMP	FSB_ACCVREF	VCCA_HPL	VCCA_HPL	VSS_D24	VSS	VSS_D22	VSS_D21	VCCA_EXP	EXP_CLKINP	EXP_CLKINN	VSS	PEG_TXP_0	D
C	VSS		FSB_SCOMPB		FSB_RCOMP		VSS_C24	VSS_C23	VSS		VSS		VCC_C18		VCCR_EXP	C
B		VSS		VCCA_MPL		VCC_B25				VSS_B21		RSVD		VSS_B17		B
A	VTT_FSB		FSB_SWING		VSS		VSS_A24	VCC3_3	VSS		VCCAPLL_EXP		VSS		PEG_RXP_0	A
	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	

Figure 12. MCH Ballout Diagram (Top View Left – Columns 15–1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
BE		VSS		DDR_A_DQ_11		VSS		DDR_A_DQ_3		VSS			VSS	NC	TEST1	BE
BD	DDR_A_DQ_22		DDR_A_DQ_16		DDR_A_DQ_14		DDR_A_DQ_8		DDR_A_DQ_6			DDR_A_DQ_1	DDR_A_DQ_4	VSS	NC	BD
BC		DDR_A_DM_2		VSS		DDR_A_DM_1	DDR_A_DQ_13	VSS		DDR_A_DQSB_0		DDR_A_DQ_0	VSS	RSVD	VSS	BC
BB	DDR_A_DQ_23	DDR_A_DQ_17	DDR_A_DQ_21	DDR_A_DQ_10	DDR_A_DQ_15	DDR_A_DQ_9		DDR_A_DQ_2	DDR_A_DQ_7		DDR_A_DM_0	DDR_A_DQ_5	VSS_BB3	VSS		BB
BA	DDR_A_DQS_2		DDR_A_DQ_20		DDR_A_DQS_1		DDR_A_DQ_12			DDR_A_DQS_0	VSS_BA5	VSS_BA4				BA
AY	DDR_A_DQSB_2		DDR_B_DQ_9	DDR_B_DQ_8	DDR_A_DQSB_1	VSS		DDR_B_DM_0	DDR_B_DQ_1	DDR_RCOMPXPD	DDR_RCOMPXPU		VSS_AY3		VSS_AY1	AY
AW	VSS		DDR_B_DQ_13	DDR_B_DQ_12	DDR_B_DQ_7	DDR_B_DQS_0		DDR_B_DQ_0	VSS	DDR_B_DQ_5		VSS		VSS_AW2		AW
AV	DDR_B_DQ_11		VSS	VSS	VSS	VSS		DDR_B_DQ_4	DDR_VREF	VSS		VSS	VSS		VSS	AV
AU											VCCA_EXP2		VSS	PEG2_TXP_14		AU
AT	DDR_B_DQ_10		DDR_B_DM_1	DDR_B_DQ_3	DDR_B_DQ_2	DDR_B_DQSB_0		VSS	DDR_RCOMPVOL	DDR_RCOMPVOH		PEG2_TXP_13	PEG2_TXN_14		VSS	AT
AR	VSS		DDR_B_DQS_1	DDR_B_DQSB_1	DDR_B_DQ_6	VCCAPLL_EXP2		VSS	VSS	VSS	PEG2_TXN_13	VSS		PEG2_TXP_12		AR
AP	DDR_B_DQ_15		VSS	RSVD	PEG2_RXN_15	PEG2_RXP_15		VSS	PEG2_TXP_15	PEG2_TXN_15		PEG2_TXP_11	VCCR_EXP		PEG2_TXN_12	AP
AN	DDR_B_DQ_14		RSVD	RSVD	DDR3_DRAM_PWROK	EXP2_COMPI		EXP2_COMPO	VSS	VSS	PEG2_TXN_11	VSS		PEG2_TXP_10		AN
AM		RSVD										PEG2_TXP_9	PEG2_TXN_10		VSS	AM
AL			CL_PWROK	VSS	PEG2_RXP_13	PEG2_RXN_13		VSS	PEG2_RXN_14	PEG2_RXP_14	PEG2_TXN_9	VSS		PEG2_TXP_8		AL
AK	CL_DATA	CL_CLK	PEG2_RXN_12	PEG2_RXP_12	VSS	VSS		VSS	VSS	VSS		PEG2_TXP_7	VCCR_EXP		PEG2_TXN_8	AK
AJ											PEG2_TXN_7	VSS		PEG2_TXP_6		AJ
AH	VCC_CL	VCC_CL	PEG2_RXN_9	VSS	PEG2_RXP_10	PEG2_RXN_10		VSS	PEG2_RXP_11	PEG2_RXN_11		PEG2_TXP_5	PEG2_TXN_6		VSS	AH
AG	VCC	CL_VREF	VSS	PEG2_RXP_9	CL_RSTB	VSS		VSS	VSS	VSS	PEG2_TXN_5	VSS		PEG2_TXP_4		AG
AF												PEG2_TXP_3	VCCR_EXP		PEG2_TXN_4	AF
AE	VCCR_EXP	EXP2_CLKINP	PEG2_RXP_6	VSS	PEG2_RXN_7	PEG2_RXP_7		VSS	PEG2_RXP_8	PEG2_RXN_8	PEG2_TXN_3	VSS		PEG2_TXP_2		AE
AD	VCCR_EXP	EXP2_CLKINN	VSS	PEG2_RXN_6	VCC_EXP	VCC_EXP		VCC_EXP	VCC_EXP	VSS		PEG2_TXP_1	PEG2_TXN_2		VSS	AD
AC	VCCR_EXP	VSS	PEG2_RXP_3	VSS	PEG2_RXP_4	PEG2_RXN_4		VSS	PEG2_RXN_5	PEG2_RXP_5		PEG2_TXN_1	VCCR_EXP		VSS	AC
AB	VCC	VCCR_EXP	VCC_EXT_PLL	PEG2_RXN_3	VCC_EXP	VCC_EXP		VCC_EXP	VCC_EXP	VCC_EXP		VCC_EXP	PEG2_TXP_0		PEG2_TXN_0	AB
AA	VCCR_EXP	VCCR_EXP	PEG2_RXN_0	VSS	PEG2_RXN_1	PEG2_RXP_1		VSS	PEG2_RXN_2	PEG2_RXP_2	VCC_EXP	VCC_EXP		VCC_EXP		AA
Y												VCC_EXP	VCC_EXP		VCC_EXP	Y
W	VCCR_EXP	VSS	VSS	PEG2_RXP_0	VCC_EXP	VCC_EXP		VCC_EXP	VCC_EXP	VSS	VCC_EXP	VCC_EXP		VCC_EXP		W
V	VCCR_EXP	VCCR_EXP	VSS	RSVD	DMI_TXN_3	DMI_TXP_3		VSS	DMI_RXP_3	DMI_RXN_3		VCC_EXP	VCC_EXP		VCC_EXP	V
U											VCC_EXP	VCC_EXP		VCC_EXP		U
T	VCCR_EXP	VCCR_EXP	VSS	RSVD	VSS	EXP_COMPO		DMI_RXN_1	DMI_RXP_1	VSS		VCC_EXP	VCC_EXP		DMI_TXN_2	T
R			VSS	VSS	VSS	EXP_COMPI		VSS	DMI_TXP_0	DMI_TXN_0	DMI_RXN_2	VSS		DMI_TXP_2		R
P		VSS										DMI_RXP_2	DMI_TXN_1		VSS	P
N	VCC_N15		PEG_RXP_4	RSVD	RSVD	PEG_RXN_15		PEG_RXP_15	VSS	VSS	DMI_RXP_0	VSS		DMI_TXP_1		N
M	VSS_M15		PEG_RXN_4	VSS	PEG_RXP_12	VSS		PEG_RXN_13	PEG_RXP_13	VSS		DMI_RXN_0	VCCR_EXP		PEG_TXP_15	M
L	VSS		PEG_RXP_3	PEG_RXN_6	VSS	PEG_RXN_12		VSS	VSS	VSS	PEG_TXP_14	VSS		PEG_TXN_15		L
K	VSS		PEG_RXN_3	VSS	PEG_RXP_6	VSS		PEG_RXN_11	PEG_RXP_11	VSS		PEG_TXN_14	PEG_RXP_14		VSS	K
J											PEG_TXP_13		VSS	PEG_RXN_14		J
H	RSVD_H15		PEG_RXP_2	PEG_RXP_5	VSS	PEG_RXN_7		VSS	VSS	VSS		PEG_TXN_13	VCCR_EXP		PEG_TXP_12	H
G	RSVD_G15		PEG_RXN_2	PEG_RXN_5	VSS	PEG_RXP_7		VSS	VSS	PEG_RXN_9		VSS		PEG_TXN_12		G
F	VSS		VSS	VSS	VSS	VSS		VSS	PEG_RXP_9	VSS	PEG_TXP_11		PEG_TXP_10		VSS	F
E	PEG_TXP_1		PEG_TXP_2		PEG_TXN_4		PEG_TXN_6			PEG_RXP_8	VSS	PEG_TXN_11				E
D	VSS	PEG_TXN_1	VSS	PEG_TXN_2	VSS	PEG_TXP_4		PEG_TXP_6	VSS		PEG_RXN_8	VSS	PEG_TXN_10	PEG_RXP_10		D
C		PEG_RXN_1		VCCR_EXP		PEG_TXN_5	VSS	VCCR_EXP		PEG_TXP_8		PEG_TXN_8	VSS	PEG_RXN_10	VSS	C
B	PEG_RXN_0		PEG_RXP_1		PEG_TXP_3		PEG_TXP_5		PEG_TXP_7			PEG_TXN_9	PEG_TXP_9	VSS	NC	B
A		VSS		PEG_TXN_3		VSS		PEG_TXN_7		VSS			VSS	TEST2		A
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
ALLZTEST	M21
BSEL0	M22
BSEL1	F21
BSEL2	F18
CL_CLK	AK14
CL_DATA	AK15
CL_PWROK	AL13
CL_RSTB	AG11
CL_VREF	AG14
DDR_A_BS_0	BC37
DDR_A_BS_1	BB36
DDR_A_BS_2	BB26
DDR_A_CASB	BB41
DDR_A_CB_0	AL33
DDR_A_CB_1	AN35
DDR_A_CB_2	AK38
DDR_A_CB_3	AK35
DDR_A_CB_4	AK33
DDR_A_CB_5	AL34
DDR_A_CB_6	AK34
DDR_A_CB_7	AK39
DDR_A_CK_0	AT33
DDR_A_CK_1	AN28
DDR_A_CK_2	AT34
DDR_A_CK_3	AV31
DDR_A_CK_4	AN27
DDR_A_CK_5	AT35
DDR_A_CKB_0	AR33
DDR_A_CKB_1	AM28
DDR_A_CKB_2	AV35
DDR_A_CKB_3	AT31
DDR_A_CKB_4	AM27
DDR_A_CKB_5	AT36
DDR_A_CKE_0	BD25
DDR_A_CKE_1	AY24
DDR_A_CKE_2	BB25
DDR_A_CKE_3	BC24
DDR_A_CSB_0	BA40
DDR_A_CSB_1	BD42
DDR_A_CSB_2	BB39

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
DDR_A_CSB_3	AY43
DDR_A_DM_0	BB5
DDR_A_DM_1	BC10
DDR_A_DM_2	BC14
DDR_A_DM_3	AP21
DDR_A_DM_4	AU44
DDR_A_DM_5	AN44
DDR_A_DM_6	AE44
DDR_A_DM_7	AB40
DDR_A_DQ_0	BC4
DDR_A_DQ_1	BD4
DDR_A_DQ_10	BB12
DDR_A_DQ_11	BE12
DDR_A_DQ_12	BA9
DDR_A_DQ_13	BC9
DDR_A_DQ_14	BD11
DDR_A_DQ_15	BB11
DDR_A_DQ_16	BD13
DDR_A_DQ_17	BB14
DDR_A_DQ_18	BB16
DDR_A_DQ_19	BE16
DDR_A_DQ_2	BB8
DDR_A_DQ_20	BA13
DDR_A_DQ_21	BB13
DDR_A_DQ_22	BD15
DDR_A_DQ_23	BB15
DDR_A_DQ_24	AN19
DDR_A_DQ_25	AY21
DDR_A_DQ_26	AN22
DDR_A_DQ_27	AT22
DDR_A_DQ_28	AV19
DDR_A_DQ_29	AW19
DDR_A_DQ_3	BE8
DDR_A_DQ_30	AN21
DDR_A_DQ_31	AW22
DDR_A_DQ_32	AV42
DDR_A_DQ_33	AU43
DDR_A_DQ_34	AR44
DDR_A_DQ_35	AR42
DDR_A_DQ_36	AW42

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
DDR_A_DQ_37	AU41
DDR_A_DQ_38	AR41
DDR_A_DQ_39	AR40
DDR_A_DQ_4	BD3
DDR_A_DQ_40	AN41
DDR_A_DQ_41	AN42
DDR_A_DQ_42	AL44
DDR_A_DQ_43	AL42
DDR_A_DQ_44	AP42
DDR_A_DQ_45	AP45
DDR_A_DQ_46	AL40
DDR_A_DQ_47	AL41
DDR_A_DQ_48	AE41
DDR_A_DQ_49	AE42
DDR_A_DQ_5	BB4
DDR_A_DQ_50	AC42
DDR_A_DQ_51	AC45
DDR_A_DQ_52	AF42
DDR_A_DQ_53	AF45
DDR_A_DQ_54	AD40
DDR_A_DQ_55	AC39
DDR_A_DQ_56	AB42
DDR_A_DQ_57	AB43
DDR_A_DQ_58	Y42
DDR_A_DQ_59	W42
DDR_A_DQ_6	BD7
DDR_A_DQ_60	AC40
DDR_A_DQ_61	AB39
DDR_A_DQ_62	AA41
DDR_A_DQ_63	Y45
DDR_A_DQ_7	BB7
DDR_A_DQ_8	BD9
DDR_A_DQ_9	BB10
DDR_A_DQS_0	BA6
DDR_A_DQS_1	BA11
DDR_A_DQS_2	BA15
DDR_A_DQS_3	AT21
DDR_A_DQS_4	AT43
DDR_A_DQS_5	AM43
DDR_A_DQS_6	AD43

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
DDR_A_DQS_7	AA42
DDR_A_DQS_8	AL38
DDR_A_DQSB_0	BC6
DDR_A_DQSB_1	AY11
DDR_A_DQSB_2	AY15
DDR_A_DQSB_3	AV21
DDR_A_DQSB_4	AT42
DDR_A_DQSB_5	AM42
DDR_A_DQSB_6	AD42
DDR_A_DQSB_7	AA44
DDR_A_DQSB_8	AL36
DDR_A_MA_0	BC36
DDR_A_MA_1	BB31
DDR_A_MA_10	BD37
DDR_A_MA_11	BD27
DDR_A_MA_12	BB27
DDR_A_MA_13	BA42
DDR_A_MA_14	BA25
DDR_A_MA_2	BB30
DDR_A_MA_3	BB29
DDR_A_MA_4	BA29
DDR_A_MA_5	BB28
DDR_A_MA_6	BD29
DDR_A_MA_7	AY27
DDR_A_MA_8	BC28
DDR_A_MA_9	BA27
DDR_A_ODT_0	BB43
DDR_A_ODT_1	AY41
DDR_A_ODT_2	BA41
DDR_A_ODT_3	AW44
DDR_A_RASB	BB38
DDR_A_WEB	BD39
DDR_B_BS_0	BB24
DDR_B_BS_1	AW23
DDR_B_BS_2	BB18
DDR_B_CASB	BB32
DDR_B_CB_0	AK45
DDR_B_CB_1	AJ44
DDR_B_CB_2	AG42
DDR_B_CB_3	AG40

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
DDR_B_CB_4	AJ42
DDR_B_CB_5	AK42
DDR_B_CB_6	AG41
DDR_B_CB_7	AG44
DDR_B_CK_0	AW30
DDR_B_CK_1	AR28
DDR_B_CK_2	AV33
DDR_B_CK_3	AR31
DDR_B_CK_4	AY30
DDR_B_CK_5	AW34
DDR_B_CKB_0	AV30
DDR_B_CKB_1	AP28
DDR_B_CKB_2	AW33
DDR_B_CKB_3	AP31
DDR_B_CKB_4	AY28
DDR_B_CKB_5	AY34
DDR_B_CKE_0	BD17
DDR_B_CKE_1	BD19
DDR_B_CKE_2	BB17
DDR_B_CKE_3	BA17
DDR_B_CSB_0	BA31
DDR_B_CSB_1	BB35
DDR_B_CSB_2	BC32
DDR_B_CSB_3	BA35
DDR_B_DM_0	AY8
DDR_B_DM_1	AT13
DDR_B_DM_2	AW16
DDR_B_DM_3	AY25
DDR_B_DM_4	AY40
DDR_B_DM_5	AN36
DDR_B_DM_6	AG35
DDR_B_DM_7	AD35
DDR_B_DQ_0	AW8
DDR_B_DQ_1	AY7
DDR_B_DQ_10	AT15
DDR_B_DQ_11	AV15
DDR_B_DQ_12	AW12
DDR_B_DQ_13	AW13
DDR_B_DQ_14	AN15
DDR_B_DQ_15	AP15

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
DDR_B_DQ_16	AY16
DDR_B_DQ_17	AV16
DDR_B_DQ_18	AP19
DDR_B_DQ_19	AT19
DDR_B_DQ_2	AT11
DDR_B_DQ_20	AN16
DDR_B_DQ_21	AR16
DDR_B_DQ_22	AT18
DDR_B_DQ_23	AR18
DDR_B_DQ_24	AW25
DDR_B_DQ_25	AV25
DDR_B_DQ_26	AT27
DDR_B_DQ_27	AV27
DDR_B_DQ_28	AN24
DDR_B_DQ_29	AP24
DDR_B_DQ_3	AT12
DDR_B_DQ_30	AT25
DDR_B_DQ_31	AP27
DDR_B_DQ_32	AY39
DDR_B_DQ_33	AW38
DDR_B_DQ_34	AT38
DDR_B_DQ_35	AT40
DDR_B_DQ_36	AY38
DDR_B_DQ_37	AW36
DDR_B_DQ_38	AV39
DDR_B_DQ_39	AV40
DDR_B_DQ_4	AV8
DDR_B_DQ_40	AR36
DDR_B_DQ_41	AP36
DDR_B_DQ_42	AP35
DDR_B_DQ_43	AN33
DDR_B_DQ_44	AV36
DDR_B_DQ_45	AR34
DDR_B_DQ_46	AN39
DDR_B_DQ_47	AN40
DDR_B_DQ_48	AH34
DDR_B_DQ_49	AG33
DDR_B_DQ_5	AW6
DDR_B_DQ_50	AE39
DDR_B_DQ_51	AE38

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
DDR_B_DQ_52	AH33
DDR_B_DQ_53	AH36
DDR_B_DQ_54	AE40
DDR_B_DQ_55	AE33
DDR_B_DQ_56	AD39
DDR_B_DQ_57	AD36
DDR_B_DQ_58	AB32
DDR_B_DQ_59	AB38
DDR_B_DQ_6	AR11
DDR_B_DQ_60	AE35
DDR_B_DQ_61	AE34
DDR_B_DQ_62	AC36
DDR_B_DQ_63	AC34
DDR_B_DQ_7	AW11
DDR_B_DQ_8	AY12
DDR_B_DQ_9	AY13
DDR_B_DQS_0	AW10
DDR_B_DQS_1	AR13
DDR_B_DQS_2	AN18
DDR_B_DQS_3	AR25
DDR_B_DQS_4	AW39
DDR_B_DQS_5	AP39
DDR_B_DQS_6	AG39
DDR_B_DQS_7	AC33
DDR_B_DQS_8	AH43
DDR_B_DQSB_0	AT10
DDR_B_DQSB_1	AR12
DDR_B_DQSB_2	AP16
DDR_B_DQSB_3	AR24
DDR_B_DQSB_4	AV38
DDR_B_DQSB_5	AP40
DDR_B_DQSB_6	AG38
DDR_B_DQSB_7	AD33
DDR_B_DQSB_8	AH42
DDR_B_MA_0	AY22
DDR_B_MA_1	BC22
DDR_B_MA_10	AW24
DDR_B_MA_11	BA19
DDR_B_MA_12	AY18
DDR_B_MA_13	BA33

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
DDR_B_MA_14	BC18
DDR_B_MA_2	BB22
DDR_B_MA_3	BA21
DDR_B_MA_4	BD21
DDR_B_MA_5	BB21
DDR_B_MA_6	BB20
DDR_B_MA_7	AY19
DDR_B_MA_8	BE20
DDR_B_MA_9	BB19
DDR_B_ODT_0	BD33
DDR_B_ODT_1	BB34
DDR_B_ODT_2	BB33
DDR_B_ODT_3	AY35
DDR_B_RASB	BD31
DDR_B_WEB	AY31
DDR_RCOMPVOH	AT6
DDR_RCOMPVOL	AT7
DDR_RCOMPXPD	AY6
DDR_RCOMPXPU	AY5
DDR_RCOMPYPD	BC42
DDR_RCOMPYPU	BB42
DDR_VREF	AV7
DDR3_A_CSB1	BB44
DDR3_A_MA0	BD35
DDR3_A_WEB	BC40
DDR3_B_ODT3	BA37
DDR3_DRAM_PWROK	AN11
DDR3_DRAMRSTB	BB23
DMI_RXN_0	M4
DMI_RXN_1	T8
DMI_RXN_2	R5
DMI_RXN_3	V6
DMI_RXP_0	N5
DMI_RXP_1	T7
DMI_RXP_2	P4
DMI_RXP_3	V7
DMI_TXN_0	R6
DMI_TXN_1	P3
DMI_TXN_2	T1

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
DMI_TXN_3	V11
DMI_TXP_0	R7
DMI_TXP_1	N2
DMI_TXP_2	R2
DMI_TXP_3	V10
EXP_CLKINN	D18
EXP_CLKINP	D19
EXP_COMPI	R10
EXP_COMPO	T10
RSVD	L18
EXP_SLR	K19
EXP2_CLKINN	AD14
EXP2_CLKINP	AE14
EXP2_COMPI	AN10
EXP2_COMPO	AN8
FSB_AB_10	R36
FSB_AB_11	N39
FSB_AB_12	N34
FSB_AB_13	N38
FSB_AB_14	R39
FSB_AB_15	K42
FSB_AB_16	R35
FSB_AB_17	T40
FSB_AB_18	T36
FSB_AB_19	T34
FSB_AB_20	T38
FSB_AB_21	P43
FSB_AB_22	W38
FSB_AB_23	V38
FSB_AB_24	V39
FSB_AB_25	W34
FSB_AB_26	V35
FSB_AB_27	W33
FSB_AB_28	V43
FSB_AB_29	AB34
FSB_AB_3	F43
FSB_AB_30	W36
FSB_AB_31	AA33
FSB_AB_32	AA35
FSB_AB_33	AA40

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
FSB_AB_34	AB35
FSB_AB_35	AA38
FSB_AB_4	M38
FSB_AB_5	M36
FSB_AB_6	K38
FSB_AB_7	L40
FSB_AB_8	N36
FSB_AB_9	N40
FSB_ACCVREF	D27
FSB_ADSB	U44
FSB_ADSTBB_0	M40
FSB_ADSTBB_1	V34
FSB_BNRB	U42
FSB_BPRIB	H38
FSB_BREQ0B	W44
FSB_CPURSTB	D35
FSB_DB_0	P42
FSB_DB_1	N41
FSB_DB_10	J41
FSB_DB_11	G42
FSB_DB_12	H45
FSB_DB_13	G44
FSB_DB_14	F41
FSB_DB_15	E42
FSB_DB_16	F38
FSB_DB_17	F39
FSB_DB_18	B43
FSB_DB_19	L36
FSB_DB_2	N44
FSB_DB_20	G38
FSB_DB_21	K35
FSB_DB_22	G36
FSB_DB_23	G35
FSB_DB_24	K34
FSB_DB_25	H33
FSB_DB_26	F33
FSB_DB_27	L34
FSB_DB_28	N33
FSB_DB_29	L33
FSB_DB_3	M42

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
FSB_DB_30	N31
FSB_DB_31	M31
FSB_DB_32	F31
FSB_DB_33	K31
FSB_DB_34	H31
FSB_DB_35	M30
FSB_DB_36	L30
FSB_DB_37	N30
FSB_DB_38	G30
FSB_DB_39	H30
FSB_DB_4	N42
FSB_DB_40	K28
FSB_DB_41	L28
FSB_DB_42	N24
FSB_DB_43	L25
FSB_DB_44	L24
FSB_DB_45	H24
FSB_DB_46	K24
FSB_DB_47	G24
FSB_DB_48	F35
FSB_DB_49	A38
FSB_DB_5	M45
FSB_DB_50	E41
FSB_DB_51	C42
FSB_DB_52	D44
FSB_DB_53	D43
FSB_DB_54	D38
FSB_DB_55	B42
FSB_DB_56	B39
FSB_DB_57	D39
FSB_DB_58	C36
FSB_DB_59	D36
FSB_DB_6	L44
FSB_DB_60	C37
FSB_DB_61	E37
FSB_DB_62	B35
FSB_DB_63	E35
FSB_DB_7	L42
FSB_DB_8	J43
FSB_DB_9	H42

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
FSB_DBSYB	T42
FSB_DEFERB	T39
FSB_DINVB_0	L41
FSB_DINVB_1	E40
FSB_DINVB_2	N28
FSB_DINVB_3	B37
FSB_DRDYB	U41
FSB_DSTBNB_0	K43
FSB_DSTBNB_1	G34
FSB_DSTBNB_2	M25
FSB_DSTBNB_3	D41
FSB_DSTBPB_0	J44
FSB_DSTBPB_1	H34
FSB_DSTBPB_2	N25
FSB_DSTBPB_3	C40
FSB_DVREF	E27
FSB_HITB	R42
FSB_HITMB	V42
FSB_LOCKB	T45
FSB_RCOMP	C26
FSB_REQB_0	C44
FSB_REQB_1	G40
FSB_REQB_2	L39
FSB_REQB_3	K36
FSB_REQB_4	H39
FSB_RSB_0	R44
FSB_RSB_1	W41
FSB_RSB_2	R41
FSB_SCOMP	D28
FSB_SCOMPB	C28
FSB_SWING	A28
FSB_TRDYB	W40
HPL_CLKINN	P30
HPL_CLKINP	P28
ICH_SYNCB	P16
MTYPE	G19
NC	BE2
NC	BD45
NC	BD1
NC	B45

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
NC	B1
NC	A44
PEG_RXN_0	B15
PEG_RXN_1	C14
PEG_RXN_10	C2
PEG_RXN_11	K8
PEG_RXN_12	L10
PEG_RXN_13	M8
PEG_RXN_14	J2
PEG_RXN_15	N10
PEG_RXN_2	G13
PEG_RXN_3	K13
PEG_RXN_4	M13
PEG_RXN_5	G12
PEG_RXN_6	L12
PEG_RXN_7	H10
PEG_RXN_8	D5
PEG_RXN_9	G6
PEG_RXP_0	A16
PEG_RXP_1	B13
PEG_RXP_10	D2
PEG_RXP_11	K7
PEG_RXP_12	M11
PEG_RXP_13	M7
PEG_RXP_14	K3
PEG_RXP_15	N8
PEG_RXP_2	H13
PEG_RXP_3	L13
PEG_RXP_4	N13
PEG_RXP_5	H12
PEG_RXP_6	K11
PEG_RXP_7	G10
PEG_RXP_8	E6
PEG_RXP_9	F7
PEG_TXN_0	E17
PEG_TXN_1	D14
PEG_TXN_10	D3
PEG_TXN_11	E4
PEG_TXN_12	G2
PEG_TXN_13	H4

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
PEG_TXN_14	K4
PEG_TXN_15	L2
PEG_TXN_2	D12
PEG_TXN_3	A12
PEG_TXN_4	E11
PEG_TXN_5	C10
PEG_TXN_6	E9
PEG_TXN_7	A8
PEG_TXN_8	C4
PEG_TXN_9	B4
PEG_TXP_0	D16
PEG_TXP_1	E15
PEG_TXP_10	F3
PEG_TXP_11	F5
PEG_TXP_12	H1
PEG_TXP_13	J5
PEG_TXP_14	L5
PEG_TXP_15	M1
PEG_TXP_2	E13
PEG_TXP_3	B11
PEG_TXP_4	D10
PEG_TXP_5	B9
PEG_TXP_6	D8
PEG_TXP_7	B7
PEG_TXP_8	C6
PEG_TXP_9	B3
PEG2_RXN_0	AA13
PEG2_RXN_1	AA11
PEG2_RXN_10	AH10
PEG2_RXN_11	AH6
PEG2_RXN_12	AK13
PEG2_RXN_13	AL10
PEG2_RXN_14	AL7
PEG2_RXN_15	AP11
PEG2_RXN_2	AA7
PEG2_RXN_3	AB12
PEG2_RXN_4	AC10
PEG2_RXN_5	AC7
PEG2_RXN_6	AD12
PEG2_RXN_7	AE11

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
PEG2_RXN_8	AE6
PEG2_RXN_9	AH13
PEG2_RXP_0	W12
PEG2_RXP_1	AA10
PEG2_RXP_10	AH11
PEG2_RXP_11	AH7
PEG2_RXP_12	AK12
PEG2_RXP_13	AL11
PEG2_RXP_14	AL6
PEG2_RXP_15	AP10
PEG2_RXP_2	AA6
PEG2_RXP_3	AC13
PEG2_RXP_4	AC11
PEG2_RXP_5	AC6
PEG2_RXP_6	AE13
PEG2_RXP_7	AE10
PEG2_RXP_8	AE7
PEG2_RXP_9	AG12
PEG2_TXN_0	AB1
PEG2_TXN_1	AC4
PEG2_TXN_10	AM3
PEG2_TXN_11	AN5
PEG2_TXN_12	AP1
PEG2_TXN_13	AR5
PEG2_TXN_14	AT3
PEG2_TXN_15	AP6
PEG2_TXN_2	AD3
PEG2_TXN_3	AE5
PEG2_TXN_4	AF1
PEG2_TXN_5	AG5
PEG2_TXN_6	AH3
PEG2_TXN_7	AJ5
PEG2_TXN_8	AK1
PEG2_TXN_9	AL5
PEG2_TXP_0	AB3
PEG2_TXP_1	AD4
PEG2_TXP_10	AN2
PEG2_TXP_11	AP4
PEG2_TXP_12	AR2
PEG2_TXP_13	AT4

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
PEG2_TXP_14	AU2
PEG2_TXP_15	AP7
PEG2_TXP_2	AE2
PEG2_TXP_3	AF4
PEG2_TXP_4	AG2
PEG2_TXP_5	AH4
PEG2_TXP_6	AJ2
PEG2_TXP_7	AK4
PEG2_TXP_8	AL2
PEG2_TXP_9	AM4
PWROK	AM19
RSTINB	AM18
RSVD	BC2
RSVD	AP34
RSVD	AP12
RSVD	AN31
RSVD	AN30
RSVD	AN25
RSVD	AN13
RSVD	AN12
RSVD	AM32
RSVD	AM25
RSVD	AM14
RSVD	AL28
RSVD	AH28
RSVD	AG32
RSVD	AG28
RSVD	AD32
RSVD	W32
RSVD	V32
RSVD	V12
RSVD	T33
RSVD	T12
RSVD	R33
RSVD	R22
RSVD	R19
RSVD	P21
RSVD	N21
RSVD	N18
RSVD	N12

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
RSVD	N11
RSVD	M16
RSVD	L19
RSVD	K22
RSVD	K21
RSVD	H21
RSVD	G22
RSVD	F19
RSVD	B19
RSVD_G15	G15
RSVD_H15	H15
RSVD_M19	M19
RSVD_P19	P19
TCEN	G21
TEST0	BE45
TEST1	BE1
TEST2	A2
TEST3	A45
VCC	AH26
VCC	AH24
VCC	AH22
VCC	AH20
VCC	AH19
VCC	AH18
VCC	AH17
VCC	AG27
VCC	AG25
VCC	AG23
VCC	AG21
VCC	AG19
VCC	AG18
VCC	AG17
VCC	AG15
VCC	AF28
VCC	AF26
VCC	AF24
VCC	AF22
VCC	AF20
VCC	AF18
VCC	AF17

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VCC	AE28
VCC	AE27
VCC	AE25
VCC	AE23
VCC	AE21
VCC	AE19
VCC	AE18
VCC	AE17
VCC	AD28
VCC	AD26
VCC	AD24
VCC	AD22
VCC	AD20
VCC	AD18
VCC	AD17
VCC	AC28
VCC	AC27
VCC	AC25
VCC	AC23
VCC	AC21
VCC	AC19
VCC	AC18
VCC	AC17
VCC	AB28
VCC	AB26
VCC	AB24
VCC	AB22
VCC	AB20
VCC	AB18
VCC	AB17
VCC	AB15
VCC	AA28
VCC	AA27
VCC	AA25
VCC	AA23
VCC	AA21
VCC	AA19
VCC	AA18
VCC	AA17
VCC	Y28

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VCC	Y26
VCC	Y24
VCC	Y22
VCC	Y20
VCC	Y18
VCC	Y17
VCC	W28
VCC	W27
VCC	W25
VCC	W23
VCC	W21
VCC	W19
VCC	W18
VCC	W17
VCC	V28
VCC	V26
VCC	V24
VCC	V22
VCC	V20
VCC	V18
VCC	V17
VCC	U28
VCC	U27
VCC	U26
VCC	U25
VCC	U24
VCC	U23
VCC	U22
VCC	U21
VCC	U20
VCC	U19
VCC	U18
VCC	U17
VCC	R18
VCC	R16
VCC_B25	B25
VCC_C18	C18
VCC_CKDDR	BE44
VCC_CKDDR	BE43
VCC_CKDDR	BD44

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VCC_CKDDR	BD43
VCC_CKDDR	BC45
VCC_CKDDR	BC44
VCC_CL	V31
VCC_CL	AM30
VCC_CL	AM23
VCC_CL	AM22
VCC_CL	AL30
VCC_CL	AL27
VCC_CL	AL25
VCC_CL	AL24
VCC_CL	AL23
VCC_CL	AL22
VCC_CL	AL21
VCC_CL	AL19
VCC_CL	AL18
VCC_CL	AL16
VCC_CL	AK31
VCC_CL	AJ29
VCC_CL	AJ28
VCC_CL	AJ27
VCC_CL	AJ26
VCC_CL	AJ25
VCC_CL	AJ24
VCC_CL	AJ23
VCC_CL	AJ22
VCC_CL	AJ21
VCC_CL	AJ20
VCC_CL	AJ19
VCC_CL	AJ18
VCC_CL	AJ17
VCC_CL	AH31
VCC_CL	AH29
VCC_CL	AH15
VCC_CL	AH14
VCC_CL	AG31
VCC_CL	AG29
VCC_CL	AF29
VCC_CL	AE31
VCC_CL	AE29

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VCC_CL	AD31
VCC_CL	AD29
VCC_CL	AC31
VCC_CL	AC29
VCC_CL	AB31
VCC_CL	AB29
VCC_CL	AA31
VCC_CL	AA29
VCC_CL	Y29
VCC_CL	W29
VCC_CL	V29
VCC_DDR	BE40
VCC_DDR	BE36
VCC_DDR	BE32
VCC_DDR	BE28
VCC_DDR	BE24
VCC_DDR	BE22
VCC_DDR	BC38
VCC_DDR	BC34
VCC_DDR	BC30
VCC_DDR	BC26
VCC_DDR	BC23
VCC_DDR	BC20
VCC_DDR	AY45
VCC_DDR	AY23
VCC_E25	E25
VCC_EXP	AD11
VCC_EXP	AD10
VCC_EXP	AD8
VCC_EXP	AD7
VCC_EXP	AB11
VCC_EXP	AB10
VCC_EXP	AB8
VCC_EXP	AB7
VCC_EXP	AB6
VCC_EXP	AB4
VCC_EXP	AA5
VCC_EXP	AA4
VCC_EXP	AA2
VCC_EXP	Y4

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VCC_EXP	Y3
VCC_EXP	Y1
VCC_EXP	W11
VCC_EXP	W10
VCC_EXP	W8
VCC_EXP	W7
VCC_EXP	W5
VCC_EXP	W4
VCC_EXP	W2
VCC_EXP	V4
VCC_EXP	V3
VCC_EXP	V1
VCC_EXP	U5
VCC_EXP	U4
VCC_EXP	U2
VCC_EXP	T4
VCC_EXP	T3
VCC_EXT_PLL	AB13
VCC_N15	N15
VCC3_3	A23
VCC3_3_G16	G16
VCC3_3_L16	L16
VCCA_EXP	D20
VCCA_EXP2	AU5
VCCA_HPL	D26
VCCA_HPL	D25
VCCA_MPL	B27
VCCAPLL_EXP	A20
VCCAPLL_EXP2	AR10
VCCAUX	U29
VCCAUX	T31
VCCAUX	R30
VCCAUX	R28
VCCAUX	R27
VCCAUX	R25
VCCAUX	R24
VCCAUX	R23
VCCR_EXP	AP3
VCCR_EXP	AK3
VCCR_EXP	AF3

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VCCR_EXP	AE15
VCCR_EXP	AD15
VCCR_EXP	AC15
VCCR_EXP	AC3
VCCR_EXP	AB14
VCCR_EXP	AA15
VCCR_EXP	AA14
VCCR_EXP	W15
VCCR_EXP	V15
VCCR_EXP	V14
VCCR_EXP	T15
VCCR_EXP	T14
VCCR_EXP	M3
VCCR_EXP	H3
VCCR_EXP	C16
VCCR_EXP	C12
VCCR_EXP	C8
VSS	B2
VSS	BE38
VSS	BE34
VSS	BE30
VSS	BE26
VSS	BE23
VSS	BE18
VSS	BE14
VSS	BE10
VSS	BE6
VSS	BE3
VSS	BD2
VSS	BC43
VSS	BC16
VSS	BC12
VSS	BC8
VSS	BC3
VSS	BC1
VSS	BB2
VSS	AY36
VSS	AY33
VSS	AY10
VSS	AW40

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VSS	AW35
VSS	AW31
VSS	AW28
VSS	AW27
VSS	AW21
VSS	AW18
VSS	AW15
VSS	AW7
VSS	AW4
VSS	AV45
VSS	AV43
VSS	AV34
VSS	AV28
VSS	AV24
VSS	AV23
VSS	AV22
VSS	AV18
VSS	AV13
VSS	AV12
VSS	AV11
VSS	AV10
VSS	AV6
VSS	AV4
VSS	AV3
VSS	AV1
VSS	AU3
VSS	AT45
VSS	AT39
VSS	AT30
VSS	AT28
VSS	AT24
VSS	AT23
VSS	AT16
VSS	AT8
VSS	AT1
VSS	AR39
VSS	AR38
VSS	AR35
VSS	AR30
VSS	AR27

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VSS	AR23
VSS	AR22
VSS	AR21
VSS	AR19
VSS	AR15
VSS	AR8
VSS	AR7
VSS	AR6
VSS	AR4
VSS	AP43
VSS	AP38
VSS	AP33
VSS	AP30
VSS	AP25
VSS	AP23
VSS	AP22
VSS	AP18
VSS	AP13
VSS	AP8
VSS	AN38
VSS	AN34
VSS	AN23
VSS	AN7
VSS	AN6
VSS	AN4
VSS	AM45
VSS	AM24
VSS	AM21
VSS	AM16
VSS	AM1
VSS	AL39
VSS	AL35
VSS	AL12
VSS	AL8
VSS	AL4
VSS	AK43
VSS	AK40
VSS	AK36
VSS	AK32
VSS	AK11
VSS	AK10
VSS	AK8
VSS	AK7
VSS	AK6
VSS	AJ41
VSS	AJ4
VSS	AH45
VSS	AH40
VSS	AH39
VSS	AH38
VSS	AH35
VSS	AH32
VSS	AH27
VSS	AH25
VSS	AH23
VSS	AH21
VSS	AH12
VSS	AH8
VSS	AH1
VSS	AG36
VSS	AG34
VSS	AG26
VSS	AG24
VSS	AG22
VSS	AG20
VSS	AG13
VSS	AG10
VSS	AG8
VSS	AG7
VSS	AG6
VSS	AG4
VSS	AF43
VSS	AF27
VSS	AF25
VSS	AF23
VSS	AF21
VSS	AF19
VSS	AE36
VSS	AE32
VSS	AE26
VSS	AE24
VSS	AE22
VSS	AE20
VSS	AE12
VSS	AE8
VSS	AE4
VSS	AD45
VSS	AD38
VSS	AD34
VSS	AD27
VSS	AD25
VSS	AD23
VSS	AD21
VSS	AD19
VSS	AD13
VSS	AD6
VSS	AD1
VSS	AC43
VSS	AC38
VSS	AC35
VSS	AC32
VSS	AC26
VSS	AC24
VSS	AC22
VSS	AC20
VSS	AC14
VSS	AC12
VSS	AC8
VSS	AC1
VSS	AB45
VSS	AB36
VSS	AB33
VSS	AB27
VSS	AB25
VSS	AB23
VSS	AB21
VSS	AB19
VSS	AA39
VSS	AA36
VSS	AA34

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VSS	AA32
VSS	AA26
VSS	AA24
VSS	AA22
VSS	AA20
VSS	AA12
VSS	AA8
VSS	Y43
VSS	Y27
VSS	Y25
VSS	Y23
VSS	Y21
VSS	Y19
VSS	W39
VSS	W35
VSS	W26
VSS	W24
VSS	W22
VSS	W20
VSS	W14
VSS	W13
VSS	W6
VSS	V45
VSS	V40
VSS	V36
VSS	V33
VSS	V27
VSS	V25
VSS	V23
VSS	V21
VSS	V19
VSS	V13
VSS	V8
VSS	T43
VSS	T35
VSS	T32
VSS	T13
VSS	T11
VSS	T6
VSS	R40

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VSS	R38
VSS	R34
VSS	R21
VSS	R13
VSS	R12
VSS	R11
VSS	R8
VSS	R4
VSS	P45
VSS	P32
VSS	P27
VSS	P25
VSS	P24
VSS	P23
VSS	P22
VSS	P18
VSS	P14
VSS	P1
VSS	N35
VSS	N27
VSS	N23
VSS	N22
VSS	N19
VSS	N16
VSS	N7
VSS	N6
VSS	N4
VSS	M43
VSS	M39
VSS	M35
VSS	M34
VSS	M33
VSS	M28
VSS	M24
VSS	M23
VSS	M18
VSS	M12
VSS	M10
VSS	M6
VSS	L38

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VSS	L35
VSS	L31
VSS	L23
VSS	L21
VSS	L15
VSS	L11
VSS	L8
VSS	L7
VSS	L6
VSS	L4
VSS	K45
VSS	K40
VSS	K39
VSS	K33
VSS	K30
VSS	K23
VSS	K18
VSS	K15
VSS	K12
VSS	K10
VSS	K6
VSS	K1
VSS	J3
VSS	H43
VSS	H40
VSS	H36
VSS	H35
VSS	H23
VSS	H22
VSS	H19
VSS	H18
VSS	H11
VSS	H8
VSS	H7
VSS	H6
VSS	G39
VSS	G33
VSS	G31
VSS	G23
VSS	G18

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VSS	G11
VSS	G8
VSS	G7
VSS	G4
VSS	F45
VSS	F40
VSS	F36
VSS	F34
VSS	F24
VSS	F23
VSS	F16
VSS	F15
VSS	F13
VSS	F12
VSS	F11
VSS	F10
VSS	F8
VSS	F6
VSS	F1
VSS	E21
VSS	E19
VSS	E5
VSS	D42
VSS	D34
VSS	D29
VSS	D23
VSS	D17
VSS	D15
VSS	D13
VSS	D11
VSS	D7
VSS	D4
VSS	C45
VSS	C43
VSS	C38
VSS	C34
VSS	C30
VSS	C22
VSS	C20
VSS	C9

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VSS	C3
VSS	C1
VSS	B44
VSS	B29
VSS	A43
VSS	A40
VSS	A36
VSS	A34
VSS	A26
VSS	A22
VSS	A18
VSS	A14
VSS	A10
VSS	A6
VSS	A3
VSS_A24	A24
VSS_AW2	AW2
VSS_AY1	AY1
VSS_AY3	AY3
VSS_B17	B17
VSS_B21	B21
VSS_BA4	BA4
VSS_BA5	BA5
VSS_BB3	BB3
VSS_C23	C23
VSS_C24	C24
VSS_D21	D21
VSS_D22	D22
VSS_D24	D24
VSS_F22	F22
VSS_H16	H16
VSS_K16	K16
VSS_M15	M15
VSS_W31	W31
VTT_FSB	M27
VTT_FSB	L27
VTT_FSB	K27
VTT_FSB	K25
VTT_FSB	H28
VTT_FSB	H27

Table 25. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VTT_FSB	H25
VTT_FSB	G28
VTT_FSB	G27
VTT_FSB	G25
VTT_FSB	F30
VTT_FSB	F28
VTT_FSB	F27
VTT_FSB	F25
VTT_FSB	E33
VTT_FSB	E31
VTT_FSB	E29
VTT_FSB	D33
VTT_FSB	D32
VTT_FSB	D31
VTT_FSB	D30
VTT_FSB	C32
VTT_FSB	B33
VTT_FSB	B31
VTT_FSB	A32
VTT_FSB	A30
XORTEST	L22

NOTE: See list of notes at beginning of chapter.

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
BE45	TEST0
BE44	VCC_CKDDR
BE43	VCC_CKDDR
BE40	VCC_DDR
BE38	VSS
BE36	VCC_DDR
BE34	VSS
BE32	VCC_DDR
BE30	VSS
BE28	VCC_DDR
BE26	VSS
BE24	VCC_DDR
BE23	VSS
BE22	VCC_DDR
BE20	DDR_B_MA_8
BE18	VSS
BE16	DDR_A_DQ_19
BE14	VSS
BE12	DDR_A_DQ_11
BE10	VSS
BE8	DDR_A_DQ_3
BE6	VSS
BE3	VSS
BE2	NC
BE1	TEST1
BD45	NC
BD44	VCC_CKDDR
BD43	VCC_CKDDR
BD42	DDR_A_CSB_1
BD39	DDR_A_WEB
BD37	DDR_A_MA_10
BD35	DDR3_A_MA0
BD33	DDR_B_ODT_0
BD31	DDR_B_RASB
BD29	DDR_A_MA_6
BD27	DDR_A_MA_11
BD25	DDR_A_CKE_0
BD21	DDR_B_MA_4
BD19	DDR_B_CKE_1
BD17	DDR_B_CKE_0
BD15	DDR_A_DQ_22
BD13	DDR_A_DQ_16
BD11	DDR_A_DQ_14
BD9	DDR_A_DQ_8
BD7	DDR_A_DQ_6
BD4	DDR_A_DQ_1
BD3	DDR_A_DQ_4
BD2	VSS
BD1	NC
BC45	VCC_CKDDR
BC44	VCC_CKDDR
BC43	VSS
BC42	DDR_RCOMPYPD
BC40	DDR3_A_WEB
BC38	VCC_DDR
BC37	DDR_A_BS_0
BC36	DDR_A_MA_0
BC34	VCC_DDR
BC32	DDR_B_CSB_2
BC30	VCC_DDR
BC28	DDR_A_MA_8
BC26	VCC_DDR
BC24	DDR_A_CKE_3
BC23	VCC_DDR
BC22	DDR_B_MA_1
BC20	VCC_DDR
BC18	DDR_B_MA_14
BC16	VSS
BC14	DDR_A_DM_2
BC12	VSS
BC10	DDR_A_DM_1
BC9	DDR_A_DQ_13
BC8	VSS
BC6	DDR_A_DQSB_0
BC4	DDR_A_DQ_0
BC3	VSS
BC2	RSVD
BC1	VSS
BB44	DDR3_A_CSB1
BB43	DDR_A_ODT_0
BB42	DDR_RCOMPYPU
BB41	DDR_A_CASB
BB39	DDR_A_CSB_2
BB38	DDR_A_RASB
BB36	DDR_A_BS_1
BB35	DDR_B_CSB_1
BB34	DDR_B_ODT_1
BB33	DDR_B_ODT_2
BB32	DDR_B_CASB
BB31	DDR_A_MA_1
BB30	DDR_A_MA_2
BB29	DDR_A_MA_3
BB28	DDR_A_MA_5
BB27	DDR_A_MA_12
BB26	DDR_A_BS_2
BB25	DDR_A_CKE_2
BB24	DDR_B_BS_0
BB23	DDR3_DRAMRST B
BB22	DDR_B_MA_2
BB21	DDR_B_MA_5
BB20	DDR_B_MA_6
BB19	DDR_B_MA_9
BB18	DDR_B_BS_2
BB17	DDR_B_CKE_2
BB16	DDR_A_DQ_18
BB15	DDR_A_DQ_23
BB14	DDR_A_DQ_17
BB13	DDR_A_DQ_21
BB12	DDR_A_DQ_10
BB11	DDR_A_DQ_15
BB10	DDR_A_DQ_9
BB8	DDR_A_DQ_2
BB7	DDR_A_DQ_7
BB5	DDR_A_DM_0
BB4	DDR_A_DQ_5
BB3	VSS_BB3
BB2	VSS
BA42	DDR_A_MA_13
BA41	DDR_A_ODT_2

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
BA40	DDR_A_CSB_0
BA37	DDR3_B_ODT3
BA35	DDR_B_CSB_3
BA33	DDR_B_MA_13
BA31	DDR_B_CSB_0
BA29	DDR_A_MA_4
BA27	DDR_A_MA_9
BA25	DDR_A_MA_14
BA21	DDR_B_MA_3
BA19	DDR_B_MA_11
BA17	DDR_B_CKE_3
BA15	DDR_A_DQS_2
BA13	DDR_A_DQ_20
BA11	DDR_A_DQS_1
BA9	DDR_A_DQ_12
BA6	DDR_A_DQS_0
BA5	VSS_BA5
BA4	VSS_BA4
AY45	VCC_DDR
AY43	DDR_A_CSB_3
AY41	DDR_A_ODT_1
AY40	DDR_B_DM_4
AY39	DDR_B_DQ_32
AY38	DDR_B_DQ_36
AY36	VSS
AY35	DDR_B_ODT_3
AY34	DDR_B_CKB_5
AY33	VSS
AY31	DDR_B_WEB
AY30	DDR_B_CK_4
AY28	DDR_B_CKB_4
AY27	DDR_A_MA_7
AY25	DDR_B_DM_3
AY24	DDR_A_CKE_1
AY23	VCC_DDR
AY22	DDR_B_MA_0
AY21	DDR_A_DQ_25
AY19	DDR_B_MA_7
AY18	DDR_B_MA_12
AY16	DDR_B_DQ_16

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AY15	DDR_A_DQSB_2
AY13	DDR_B_DQ_9
AY12	DDR_B_DQ_8
AY11	DDR_A_DQSB_1
AY10	VSS
AY8	DDR_B_DM_0
AY7	DDR_B_DQ_1
AY6	DDR_RCOMPXPD
AY5	DDR_RCOMPXPU
AY3	VSS_AY3
AY1	VSS_AY1
AW44	DDR_A_ODT_3
AW42	DDR_A_DQ_36
AW40	VSS
AW39	DDR_B_DQS_4
AW38	DDR_B_DQ_33
AW36	DDR_B_DQ_37
AW35	VSS
AW34	DDR_B_CK_5
AW33	DDR_B_CKB_2
AW31	VSS
AW30	DDR_B_CK_0
AW28	VSS
AW27	VSS
AW25	DDR_B_DQ_24
AW24	DDR_B_MA_10
AW23	DDR_B_BS_1
AW22	DDR_A_DQ_31
AW21	VSS
AW19	DDR_A_DQ_29
AW18	VSS
AW16	DDR_B_DM_2
AW15	VSS
AW13	DDR_B_DQ_13
AW12	DDR_B_DQ_12
AW11	DDR_B_DQ_7
AW10	DDR_B_DQS_0
AW8	DDR_B_DQ_0
AW7	VSS
AW6	DDR_B_DQ_5

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AW4	VSS
AW2	VSS_AW2
AV45	VSS
AV43	VSS
AV42	DDR_A_DQ_32
AV40	DDR_B_DQ_39
AV39	DDR_B_DQ_38
AV38	DDR_B_DQSB_4
AV36	DDR_B_DQ_44
AV35	DDR_A_CKB_2
AV34	VSS
AV33	DDR_B_CK_2
AV31	DDR_A_CK_3
AV30	DDR_B_CKB_0
AV28	VSS
AV27	DDR_B_DQ_27
AV25	DDR_B_DQ_25
AV24	VSS
AV23	VSS
AV22	VSS
AV21	DDR_A_DQSB_3
AV19	DDR_A_DQ_28
AV18	VSS
AV16	DDR_B_DQ_17
AV15	DDR_B_DQ_11
AV13	VSS
AV12	VSS
AV11	VSS
AV10	VSS
AV8	DDR_B_DQ_4
AV7	DDR_VREF
AV6	VSS
AV4	VSS
AV3	VSS
AV1	VSS
AU44	DDR_A_DM_4
AU43	DDR_A_DQ_33
AU41	DDR_A_DQ_37
AU5	VCCA_EXP2
AU3	VSS

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AU2	PEG2_TXP_14
AT45	VSS
AT43	DDR_A_DQS_4
AT42	DDR_A_DQSB_4
AT40	DDR_B_DQ_35
AT39	VSS
AT38	DDR_B_DQ_34
AT36	DDR_A_CKB_5
AT35	DDR_A_CK_5
AT34	DDR_A_CK_2
AT33	DDR_A_CK_0
AT31	DDR_A_CKB_3
AT30	VSS
AT28	VSS
AT27	DDR_B_DQ_26
AT25	DDR_B_DQ_30
AT24	VSS
AT23	VSS
AT22	DDR_A_DQ_27
AT21	DDR_A_DQS_3
AT19	DDR_B_DQ_19
AT18	DDR_B_DQ_22
AT16	VSS
AT15	DDR_B_DQ_10
AT13	DDR_B_DM_1
AT12	DDR_B_DQ_3
AT11	DDR_B_DQ_2
AT10	DDR_B_DQSB_0
AT8	VSS
AT7	DDR_RCOMPVOL
AT6	DDR_RCOMPVOH
AT4	PEG2_TXP_13
AT3	PEG2_TXN_14
AT1	VSS
AR44	DDR_A_DQ_34
AR42	DDR_A_DQ_35
AR41	DDR_A_DQ_38
AR40	DDR_A_DQ_39
AR39	VSS
AR38	VSS

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AR36	DDR_B_DQ_40
AR35	VSS
AR34	DDR_B_DQ_45
AR33	DDR_A_CKB_0
AR31	DDR_B_CK_3
AR30	VSS
AR28	DDR_B_CK_1
AR27	VSS
AR25	DDR_B_DQS_3
AR24	DDR_B_DQSB_3
AR23	VSS
AR22	VSS
AR21	VSS
AR19	VSS
AR18	DDR_B_DQ_23
AR16	DDR_B_DQ_21
AR15	VSS
AR13	DDR_B_DQS_1
AR12	DDR_B_DQSB_1
AR11	DDR_B_DQ_6
AR10	VCCAPLL_EXP2
AR8	VSS
AR7	VSS
AR6	VSS
AR5	PEG2_TXN_13
AR4	VSS
AR2	PEG2_TXP_12
AP45	DDR_A_DQ_45
AP43	VSS
AP42	DDR_A_DQ_44
AP40	DDR_B_DQSB_5
AP39	DDR_B_DQS_5
AP38	VSS
AP36	DDR_B_DQ_41
AP35	DDR_B_DQ_42
AP34	RSVD
AP33	VSS
AP31	DDR_B_CKB_3
AP30	VSS
AP28	DDR_B_CKB_1

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AP27	DDR_B_DQ_31
AP25	VSS
AP24	DDR_B_DQ_29
AP23	VSS
AP22	VSS
AP21	DDR_A_DM_3
AP19	DDR_B_DQ_18
AP18	VSS
AP16	DDR_B_DQSB_2
AP15	DDR_B_DQ_15
AP13	VSS
AP12	RSVD
AP11	PEG2_RXN_15
AP10	PEG2_RXP_15
AP8	VSS
AP7	PEG2_TXP_15
AP6	PEG2_TXN_15
AP4	PEG2_TXP_11
AP3	VCCR_EXP
AP1	PEG2_TXN_12
AN44	DDR_A_DM_5
AN42	DDR_A_DQ_41
AN41	DDR_A_DQ_40
AN40	DDR_B_DQ_47
AN39	DDR_B_DQ_46
AN38	VSS
AN36	DDR_B_DM_5
AN35	DDR_A_CB_1
AN34	VSS
AN33	DDR_B_DQ_43
AN31	RSVD
AN30	RSVD
AN28	DDR_A_CK_1
AN27	DDR_A_CK_4
AN25	RSVD
AN24	DDR_B_DQ_28
AN23	VSS
AN22	DDR_A_DQ_26
AN21	DDR_A_DQ_30
AN19	DDR_A_DQ_24

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AN18	DDR_B_DQS_2
AN16	DDR_B_DQ_20
AN15	DDR_B_DQ_14
AN13	RSVD
AN12	RSVD
AN11	DDR3_DRAM_PWROK
AN10	EXP2_COMPI
AN8	EXP2_COMPO
AN7	VSS
AN6	VSS
AN5	PEG2_TXN_11
AN4	VSS
AN2	PEG2_TXP_10
AM45	VSS
AM43	DDR_A_DQS_5
AM42	DDR_A_DQSB_5
AM32	RSVD
AM30	VCC_CL
AM28	DDR_A_CKB_1
AM27	DDR_A_CKB_4
AM25	RSVD
AM24	VSS
AM23	VCC_CL
AM22	VCC_CL
AM21	VSS
AM19	PWROK
AM18	RSTINB
AM16	VSS
AM14	RSVD
AM4	PEG2_TXP_9
AM3	PEG2_TXN_10
AM1	VSS
AL44	DDR_A_DQ_42
AL42	DDR_A_DQ_43
AL41	DDR_A_DQ_47
AL40	DDR_A_DQ_46
AL39	VSS
AL38	DDR_A_DQS_8
AL36	DDR_A_DQSB_8

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AL35	VSS
AL34	DDR_A_CB_5
AL33	DDR_A_CB_0
AL30	VCC_CL
AL28	RSVD
AL27	VCC_CL
AL25	VCC_CL
AL24	VCC_CL
AL23	VCC_CL
AL22	VCC_CL
AL21	VCC_CL
AL19	VCC_CL
AL18	VCC_CL
AL16	VCC_CL
AL13	CL_PWROK
AL12	VSS
AL11	PEG2_RXP_13
AL10	PEG2_RXN_13
AL8	VSS
AL7	PEG2_RXN_14
AL6	PEG2_RXP_14
AL5	PEG2_TXN_9
AL4	VSS
AL2	PEG2_TXP_8
AK45	DDR_B_CB_0
AK43	VSS
AK42	DDR_B_CB_5
AK40	VSS
AK39	DDR_A_CB_7
AK38	DDR_A_CB_2
AK36	VSS
AK35	DDR_A_CB_3
AK34	DDR_A_CB_6
AK33	DDR_A_CB_4
AK32	VSS
AK31	VCC_CL
AK15	CL_DATA
AK14	CL_CLK
AK13	PEG2_RXN_12
AK12	PEG2_RXP_12

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AK11	VSS
AK10	VSS
AK8	VSS
AK7	VSS
AK6	VSS
AK4	PEG2_TXP_7
AK3	VCCR_EXP
AK1	PEG2_TXN_8
AJ44	DDR_B_CB_1
AJ42	DDR_B_CB_4
AJ41	VSS
AJ29	VCC_CL
AJ28	VCC_CL
AJ27	VCC_CL
AJ26	VCC_CL
AJ25	VCC_CL
AJ24	VCC_CL
AJ23	VCC_CL
AJ22	VCC_CL
AJ21	VCC_CL
AJ20	VCC_CL
AJ19	VCC_CL
AJ18	VCC_CL
AJ17	VCC_CL
AJ5	PEG2_TXN_7
AJ4	VSS
AJ2	PEG2_TXP_6
AH45	VSS
AH43	DDR_B_DQS_8
AH42	DDR_B_DQSB_8
AH40	VSS
AH39	VSS
AH38	VSS
AH36	DDR_B_DQ_53
AH35	VSS
AH34	DDR_B_DQ_48
AH33	DDR_B_DQ_52
AH32	VSS
AH31	VCC_CL
AH29	VCC_CL

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AH28	RSVD
AH27	VSS
AH26	VCC
AH25	VSS
AH24	VCC
AH23	VSS
AH22	VCC
AH21	VSS
AH20	VCC
AH19	VCC
AH18	VCC
AH17	VCC
AH15	VCC_CL
AH14	VCC_CL
AH13	PEG2_RXN_9
AH12	VSS
AH11	PEG2_RXP_10
AH10	PEG2_RXN_10
AH8	VSS
AH7	PEG2_RXP_11
AH6	PEG2_RXN_11
AH4	PEG2_TXP_5
AH3	PEG2_TXN_6
AH1	VSS
AG44	DDR_B_CB_7
AG42	DDR_B_CB_2
AG41	DDR_B_CB_6
AG40	DDR_B_CB_3
AG39	DDR_B_DQS_6
AG38	DDR_B_DQSB_6
AG36	VSS
AG35	DDR_B_DM_6
AG34	VSS
AG33	DDR_B_DQ_49
AG32	RSVD
AG31	VCC_CL
AG29	VCC_CL
AG28	RSVD
AG27	VCC
AG26	VSS

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AG25	VCC
AG24	VSS
AG23	VCC
AG22	VSS
AG21	VCC
AG20	VSS
AG19	VCC
AG18	VCC
AG17	VCC
AG15	VCC
AG14	CL_VREF
AG13	VSS
AG12	PEG2_RXP_9
AG11	CL_RSTB
AG10	VSS
AG8	VSS
AG7	VSS
AG6	VSS
AG5	PEG2_TXN_5
AG4	VSS
AG2	PEG2_TXP_4
AF45	DDR_A_DQ_53
AF43	VSS
AF42	DDR_A_DQ_52
AF29	VCC_CL
AF28	VCC
AF27	VSS
AF26	VCC
AF25	VSS
AF24	VCC
AF23	VSS
AF22	VCC
AF21	VSS
AF20	VCC
AF19	VSS
AF18	VCC
AF17	VCC
AF4	PEG2_TXP_3
AF3	VCCR_EXP
AF1	PEG2_TXN_4

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AE44	DDR_A_DM_6
AE42	DDR_A_DQ_49
AE41	DDR_A_DQ_48
AE40	DDR_B_DQ_54
AE39	DDR_B_DQ_50
AE38	DDR_B_DQ_51
AE36	VSS
AE35	DDR_B_DQ_60
AE34	DDR_B_DQ_61
AE33	DDR_B_DQ_55
AE32	VSS
AE31	VCC_CL
AE29	VCC_CL
AE28	VCC
AE27	VCC
AE26	VSS
AE25	VCC
AE24	VSS
AE23	VCC
AE22	VSS
AE21	VCC
AE20	VSS
AE19	VCC
AE18	VCC
AE17	VCC
AE15	VCCR_EXP
AE14	EXP2_CLKINP
AE13	PEG2_RXP_6
AE12	VSS
AE11	PEG2_RXN_7
AE10	PEG2_RXP_7
AE8	VSS
AE7	PEG2_RXP_8
AE6	PEG2_RXN_8
AE5	PEG2_TXN_3
AE4	VSS
AE2	PEG2_TXP_2
AD45	VSS
AD43	DDR_A_DQS_6
AD42	DDR_A_DQSB_6

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AD40	DDR_A_DQ_54
AD39	DDR_B_DQ_56
AD38	VSS
AD36	DDR_B_DQ_57
AD35	DDR_B_DM_7
AD34	VSS
AD33	DDR_B_DQSB_7
AD32	RSVD
AD31	VCC_CL
AD29	VCC_CL
AD28	VCC
AD27	VSS
AD26	VCC
AD25	VSS
AD24	VCC
AD23	VSS
AD22	VCC
AD21	VSS
AD20	VCC
AD19	VSS
AD18	VCC
AD17	VCC
AD15	VCCR_EXP
AD14	EXP2_CLKINN
AD13	VSS
AD12	PEG2_RXN_6
AD11	VCC_EXP
AD10	VCC_EXP
AD8	VCC_EXP
AD7	VCC_EXP
AD6	VSS
AD4	PEG2_TXP_1
AD3	PEG2_TXN_2
AD1	VSS
AC45	DDR_A_DQ_51
AC43	VSS
AC42	DDR_A_DQ_50
AC40	DDR_A_DQ_60
AC39	DDR_A_DQ_55
AC38	VSS

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AC36	DDR_B_DQ_62
AC35	VSS
AC34	DDR_B_DQ_63
AC33	DDR_B_DQS_7
AC32	VSS
AC31	VCC_CL
AC29	VCC_CL
AC28	VCC
AC27	VCC
AC26	VSS
AC25	VCC
AC24	VSS
AC23	VCC
AC22	VSS
AC21	VCC
AC20	VSS
AC19	VCC
AC18	VCC
AC17	VCC
AC15	VCCR_EXP
AC14	VSS
AC13	PEG2_RXP_3
AC12	VSS
AC11	PEG2_RXP_4
AC10	PEG2_RXN_4
AC8	VSS
AC7	PEG2_RXN_5
AC6	PEG2_RXP_5
AC4	PEG2_TXN_1
AC3	VCCR_EXP
AC1	VSS
AB45	VSS
AB43	DDR_A_DQ_57
AB42	DDR_A_DQ_56
AB40	DDR_A_DM_7
AB39	DDR_A_DQ_61
AB38	DDR_B_DQ_59
AB36	VSS
AB35	FSB_AB_34
AB34	FSB_AB_29

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AB33	VSS
AB32	DDR_B_DQ_58
AB31	VCC_CL
AB29	VCC_CL
AB28	VCC
AB27	VSS
AB26	VCC
AB25	VSS
AB24	VCC
AB23	VSS
AB22	VCC
AB21	VSS
AB20	VCC
AB19	VSS
AB18	VCC
AB17	VCC
AB15	VCC
AB14	VCCR_EXP
AB13	VCC_EXT_PLL
AB12	PEG2_RXN_3
AB11	VCC_EXP
AB10	VCC_EXP
AB8	VCC_EXP
AB7	VCC_EXP
AB6	VCC_EXP
AB4	VCC_EXP
AB3	PEG2_TXP_0
AB1	PEG2_TXN_0
AA44	DDR_A_DQSB_7
AA42	DDR_A_DQS_7
AA41	DDR_A_DQ_62
AA40	FSB_AB_33
AA39	VSS
AA38	FSB_AB_35
AA36	VSS
AA35	FSB_AB_32
AA34	VSS
AA33	FSB_AB_31
AA32	VSS
AA31	VCC_CL

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AA29	VCC_CL
AA28	VCC
AA27	VCC
AA26	VSS
AA25	VCC
AA24	VSS
AA23	VCC
AA22	VSS
AA21	VCC
AA20	VSS
AA19	VCC
AA18	VCC
AA17	VCC
AA15	VCCR_EXP
AA14	VCCR_EXP
AA13	PEG2_RXN_0
AA12	VSS
AA11	PEG2_RXN_1
AA10	PEG2_RXP_1
AA8	VSS
AA7	PEG2_RXN_2
AA6	PEG2_RXP_2
AA5	VCC_EXP
AA4	VCC_EXP
AA2	VCC_EXP
Y45	DDR_A_DQ_63
Y43	VSS
Y42	DDR_A_DQ_58
Y29	VCC_CL
Y28	VCC
Y27	VSS
Y26	VCC
Y25	VSS
Y24	VCC
Y23	VSS
Y22	VCC
Y21	VSS
Y20	VCC
Y19	VSS
Y18	VCC

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
Y17	VCC
Y4	VCC_EXP
Y3	VCC_EXP
Y1	VCC_EXP
W44	FSB_BREQ0B
W42	DDR_A_DQ_59
W41	FSB_RSB_1
W40	FSB_TRDYB
W39	VSS
W38	FSB_AB_22
W36	FSB_AB_30
W35	VSS
W34	FSB_AB_25
W33	FSB_AB_27
W32	RSVD
W31	VSS_W31
W29	VCC_CL
W28	VCC
W27	VCC
W26	VSS
W25	VCC
W24	VSS
W23	VCC
W22	VSS
W21	VCC
W20	VSS
W19	VCC
W18	VCC
W17	VCC
W15	VCCR_EXP
W14	VSS
W13	VSS
W12	PEG2_RXP_0
W11	VCC_EXP
W10	VCC_EXP
W8	VCC_EXP
W7	VCC_EXP
W6	VSS
W5	VCC_EXP
W4	VCC_EXP

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
W2	VCC_EXP
V45	VSS
V43	FSB_AB_28
V42	FSB_HITMB
V40	VSS
V39	FSB_AB_24
V38	FSB_AB_23
V36	VSS
V35	FSB_AB_26
V34	FSB_ADSTBB_1
V33	VSS
V32	RSVD
V31	VCC_CL
V29	VCC_CL
V28	VCC
V27	VSS
V26	VCC
V25	VSS
V24	VCC
V23	VSS
V22	VCC
V21	VSS
V20	VCC
V19	VSS
V18	VCC
V17	VCC
V15	VCCR_EXP
V14	VCCR_EXP
V13	VSS
V12	RSVD
V11	DMI_TXN_3
V10	DMI_TXP_3
V8	VSS
V7	DMI_RXP_3
V6	DMI_RXN_3
V4	VCC_EXP
V3	VCC_EXP
V1	VCC_EXP
U44	FSB_ADSB
U42	FSB_BNRB

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
U41	FSB_DRDYB
U29	VCCAUX
U28	VCC
U27	VCC
U26	VCC
U25	VCC
U24	VCC
U23	VCC
U22	VCC
U21	VCC
U20	VCC
U19	VCC
U18	VCC
U17	VCC
U5	VCC_EXP
U4	VCC_EXP
U2	VCC_EXP
T45	FSB_LOCKB
T43	VSS
T42	FSB_DBSYB
T40	FSB_AB_17
T39	FSB_DEFERB
T38	FSB_AB_20
T36	FSB_AB_18
T35	VSS
T34	FSB_AB_19
T33	RSVD
T32	VSS
T31	VCCAUX
T15	VCCR_EXP
T14	VCCR_EXP
T13	VSS
T12	RSVD
T11	VSS
T10	EXP_COMPO
T8	DMI_RXN_1
T7	DMI_RXP_1
T6	VSS
T4	VCC_EXP
T3	VCC_EXP

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
T1	DMI_TXN_2
R44	FSB_RSB_0
R42	FSB_HITB
R41	FSB_RSB_2
R40	VSS
R39	FSB_AB_14
R38	VSS
R36	FSB_AB_10
R35	FSB_AB_16
R34	VSS
R33	RSVD
R30	VCCAUX
R28	VCCAUX
R27	VCCAUX
R25	VCCAUX
R24	VCCAUX
R23	VCCAUX
R22	RSVD
R21	VSS
R19	RSVD
R18	VCC
R16	VCC
R13	VSS
R12	VSS
R11	VSS
R10	EXP_COMPI
R8	VSS
R7	DMI_TXP_0
R6	DMI_TXN_0
R5	DMI_RXN_2
R4	VSS
R2	DMI_TXP_2
P45	VSS
P43	FSB_AB_21
P42	FSB_DB_0
P32	VSS
P30	HPL_CLKINN
P28	HPL_CLKINP
P27	VSS
P25	VSS

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
P24	VSS
P23	VSS
P22	VSS
P21	RSVD
P19	RSVD_P19
P18	VSS
P16	ICH_SYNCB
P14	VSS
P4	DMI_RXP_2
P3	DMI_TXN_1
P1	VSS
N44	FSB_DB_2
N42	FSB_DB_4
N41	FSB_DB_1
N40	FSB_AB_9
N39	FSB_AB_11
N38	FSB_AB_13
N36	FSB_AB_8
N35	VSS
N34	FSB_AB_12
N33	FSB_DB_28
N31	FSB_DB_30
N30	FSB_DB_37
N28	FSB_DINVB_2
N27	VSS
N25	FSB_DSTBPB_2
N24	FSB_DB_42
N23	VSS
N22	VSS
N21	RSVD
N19	VSS
N18	RSVD
N16	VSS
N15	VCC_N15
N13	PEG_RXP_4
N12	RSVD
N11	RSVD
N10	PEG_RXN_15
N8	PEG_RXP_15
N7	VSS

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
N6	VSS
N5	DMI_RXP_0
N4	VSS
N2	DMI_TXP_1
M45	FSB_DB_5
M43	VSS
M42	FSB_DB_3
M40	FSB_ADSTBB_0
M39	VSS
M38	FSB_AB_4
M36	FSB_AB_5
M35	VSS
M34	VSS
M33	VSS
M31	FSB_DB_31
M30	FSB_DB_35
M28	VSS
M27	VTT_FSB
M25	FSB_DSTBNB_2
M24	VSS
M23	VSS
M22	BSEL0
M21	ALLZTEST
M19	RSVD_M19
M18	VSS
M16	RSVD
M15	VSS_M15
M13	PEG_RXN_4
M12	VSS
M11	PEG_RXP_12
M10	VSS
M8	PEG_RXN_13
M7	PEG_RXP_13
M6	VSS
M4	DMI_RXN_0
M3	VCCR_EXP
M1	PEG_TXP_15
L44	FSB_DB_6
L42	FSB_DB_7
L41	FSB_DINVB_0

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
L40	FSB_AB_7
L39	FSB_REQB_2
L38	VSS
L36	FSB_DB_19
L35	VSS
L34	FSB_DB_27
L33	FSB_DB_29
L31	VSS
L30	FSB_DB_36
L28	FSB_DB_41
L27	VTT_FSB
L25	FSB_DB_43
L24	FSB_DB_44
L23	VSS
L22	XORTEST
L21	VSS
L19	RSVD
L18	RSVD
L16	VCC3_3_L16
L15	VSS
L13	PEG_RXP_3
L12	PEG_RXN_6
L11	VSS
L10	PEG_RXN_12
L8	VSS
L7	VSS
L6	VSS
L5	PEG_TXP_14
L4	VSS
L2	PEG_TXN_15
K45	VSS
K43	FSB_DSTBNB_0
K42	FSB_AB_15
K40	VSS
K39	VSS
K38	FSB_AB_6
K36	FSB_REQB_3
K35	FSB_DB_21
K34	FSB_DB_24
K33	VSS

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
K31	FSB_DB_33
K30	VSS
K28	FSB_DB_40
K27	VTT_FSB
K25	VTT_FSB
K24	FSB_DB_46
K23	VSS
K22	RSVD
K21	RSVD
K19	EXP_SLR
K18	VSS
K16	VSS_K16
K15	VSS
K13	PEG_RXN_3
K12	VSS
K11	PEG_RXP_6
K10	VSS
K8	PEG_RXN_11
K7	PEG_RXP_11
K6	VSS
K4	PEG_TXN_14
K3	PEG_RXP_14
K1	VSS
J44	FSB_DSTBPB_0
J43	FSB_DB_8
J41	FSB_DB_10
J5	PEG_TXP_13
J3	VSS
J2	PEG_RXN_14
H45	FSB_DB_12
H43	VSS
H42	FSB_DB_9
H40	VSS
H39	FSB_REQB_4
H38	FSB_BPRIB
H36	VSS
H35	VSS
H34	FSB_DSTBPB_1
H33	FSB_DB_25
H31	FSB_DB_34

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
H30	FSB_DB_39
H28	VTT_FSB
H27	VTT_FSB
H25	VTT_FSB
H24	FSB_DB_45
H23	VSS
H22	VSS
H21	RSVD
H19	VSS
H18	VSS
H16	VSS_H16
H15	RSVD_H15
H13	PEG_RXP_2
H12	PEG_RXP_5
H11	VSS
H10	PEG_RXN_7
H8	VSS
H7	VSS
H6	VSS
H4	PEG_TXN_13
H3	VCCR_EXP
H1	PEG_TXP_12
G44	FSB_DB_13
G42	FSB_DB_11
G40	FSB_REQB_1
G39	VSS
G38	FSB_DB_20
G36	FSB_DB_22
G35	FSB_DB_23
G34	FSB_DSTBNB_1
G33	VSS
G31	VSS
G30	FSB_DB_38
G28	VTT_FSB
G27	VTT_FSB
G25	VTT_FSB
G24	FSB_DB_47
G23	VSS
G22	RSVD
G21	TCEN

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
G19	MTYPE
G18	VSS
G16	VCC3_3_G16
G15	RSVD_G15
G13	PEG_RXN_2
G12	PEG_RXN_5
G11	VSS
G10	PEG_RXP_7
G8	VSS
G7	VSS
G6	PEG_RXN_9
G4	VSS
G2	PEG_TXN_12
F45	VSS
F43	FSB_AB_3
F41	FSB_DB_14
F40	VSS
F39	FSB_DB_17
F38	FSB_DB_16
F36	VSS
F35	FSB_DB_48
F34	VSS
F33	FSB_DB_26
F31	FSB_DB_32
F30	VTT_FSB
F28	VTT_FSB
F27	VTT_FSB
F25	VTT_FSB
F24	VSS
F23	VSS
F22	VSS_F22
F21	BSEL1
F19	RSVD
F18	BSEL2
F16	VSS
F15	VSS
F13	VSS
F12	VSS
F11	VSS
F10	VSS

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
F8	VSS
F7	PEG_RXP_9
F6	VSS
F5	PEG_TXP_11
F3	PEG_TXP_10
F1	VSS
E42	FSB_DB_15
E41	FSB_DB_50
E40	FSB_DINVB_1
E37	FSB_DB_61
E35	FSB_DB_63
E33	VTT_FSB
E31	VTT_FSB
E29	VTT_FSB
E27	FSB_DVREF
E25	VCC_E25
E21	VSS
E19	VSS
E17	PEG_TXN_0
E15	PEG_TXP_1
E13	PEG_TXP_2
E11	PEG_TXN_4
E9	PEG_TXN_6
E6	PEG_RXP_8
E5	VSS
E4	PEG_TXN_11
D44	FSB_DB_52
D43	FSB_DB_53
D42	VSS
D41	FSB_DSTBNB_3
D39	FSB_DB_57
D38	FSB_DB_54
D36	FSB_DB_59
D35	FSB_CPURSTB
D34	VSS
D33	VTT_FSB
D32	VTT_FSB
D31	VTT_FSB
D30	VTT_FSB
D29	VSS

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
D28	FSB_SCOMP
D27	FSB_ACCVREF
D26	VCCA_HPL
D25	VCCA_HPL
D24	VSS_D24
D23	VSS
D22	VSS_D22
D21	VSS_D21
D20	VCCA_EXP
D19	EXP_CLKINP
D18	EXP_CLKINN
D17	VSS
D16	PEG_TXP_0
D15	VSS
D14	PEG_TXN_1
D13	VSS
D12	PEG_TXN_2
D11	VSS
D10	PEG_TXP_4
D8	PEG_TXP_6
D7	VSS
D5	PEG_RXN_8
D4	VSS
D3	PEG_TXN_10
D2	PEG_RXP_10
C45	VSS
C44	FSB_REQB_0
C43	VSS
C42	FSB_DB_51
C40	FSB_DSTBPB_3
C38	VSS
C37	FSB_DB_60
C36	FSB_DB_58
C34	VSS
C32	VTT_FSB
C30	VSS
C28	FSB_SCOMPB
C26	FSB_RCOMP
C24	VSS_C24
C23	VSS_C23

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
C22	VSS
C20	VSS
C18	VCC_C18
C16	VCCR_EXP
C14	PEG_RXN_1
C12	VCCR_EXP
C10	PEG_TXN_5
C9	VSS
C8	VCCR_EXP
C6	PEG_TXP_8
C4	PEG_TXN_8
C3	VSS
C2	PEG_RXN_10
C1	VSS
B45	NC
B44	VSS
B43	FSB_DB_18
B42	FSB_DB_55
B39	FSB_DB_56
B37	FSB_DINVB_3
B35	FSB_DB_62
B33	VTT_FSB
B31	VTT_FSB
B29	VSS
B27	VCCA_MPL
B25	VCC_B25
B21	VSS_B21
B19	RSVD
B17	VSS_B17
B15	PEG_RXN_0
B13	PEG_RXP_1
B11	PEG_TXP_3
B9	PEG_TXP_5
B7	PEG_TXP_7
B4	PEG_TXN_9
B3	PEG_TXP_9
B2	VSS
B1	NC
A45	TEST3
A44	NC

Table 26. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
A43	VSS
A40	VSS
A38	FSB_DB_49
A36	VSS
A34	VSS
A32	VTT_FSB
A30	VTT_FSB
A28	FSB_SWING
A26	VSS
A24	VSS_A24
A23	VCC3_3
A22	VSS
A20	VCCAPLL_EXP
A18	VSS
A16	PEG_RXP_0
A14	VSS
A12	PEG_TXN_3
A10	VSS
A8	PEG_TXN_7
A6	VSS
A3	VSS
A2	TEST2

NOTE: See list of notes at beginning of chapter.

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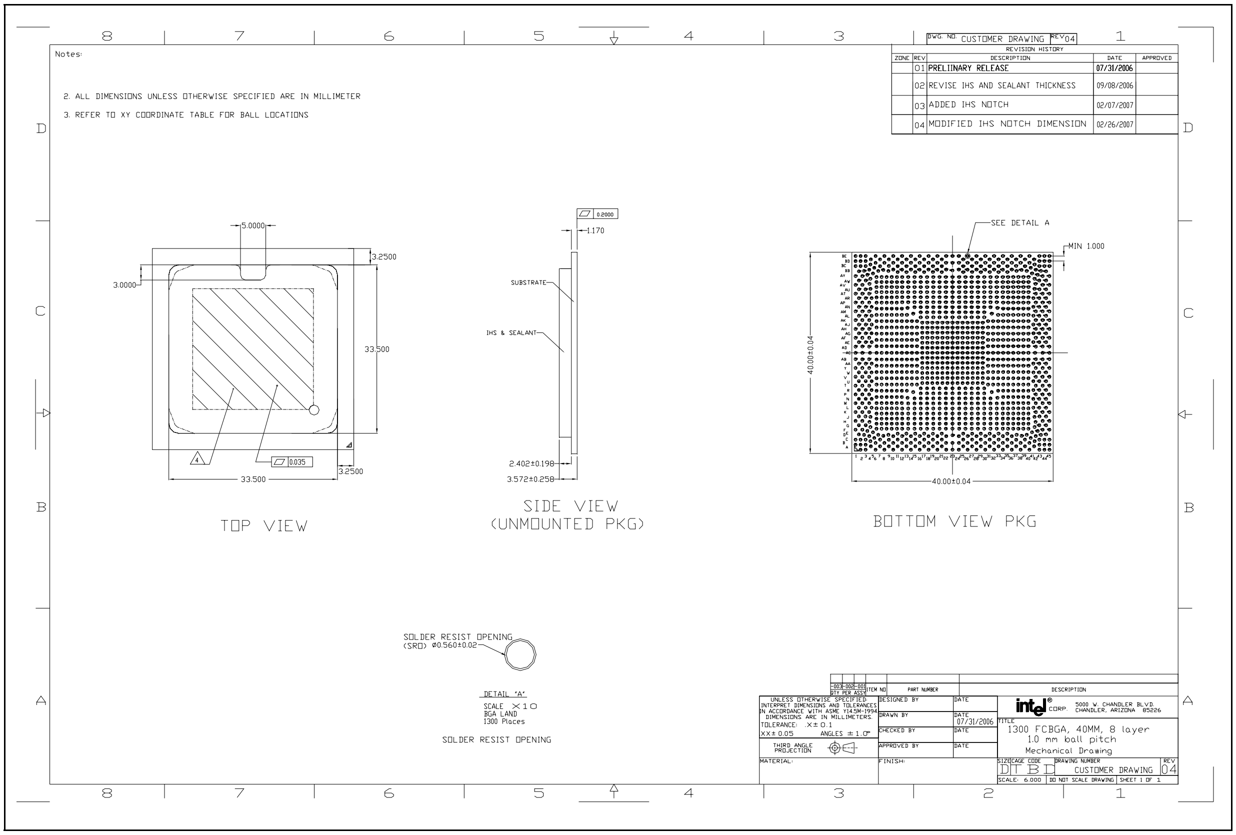
11.2 Package Information

The MCH is available in a 40 mm [1.57 in] x 40 mm [1.57 in] Flip Chip Ball Grid Array (FC-BGA) package with an integrated heat spreader (IHS) and 1300 solder balls. Figure 13 shows the package drawing.

Figure 13. MCH Package Drawing



12 Testability

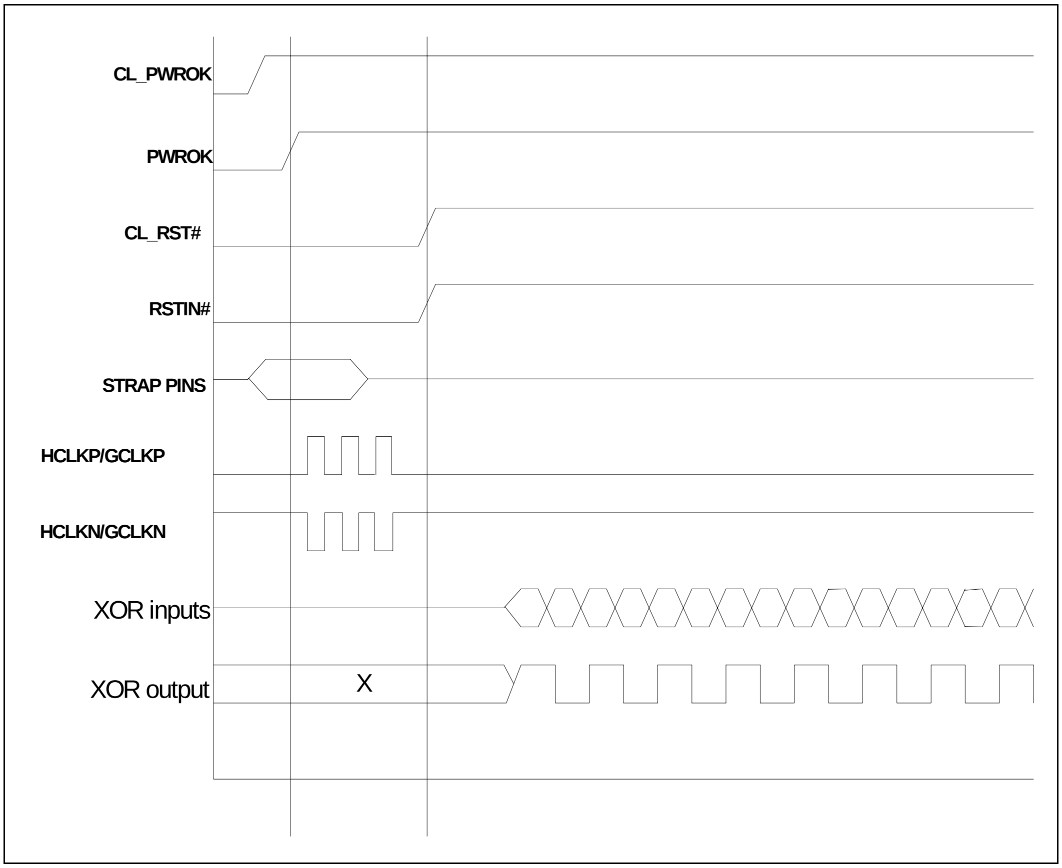
In the MCH, testability for Automated Test Equipment (ATE) board level testing has been implemented as an XOR chain. An XOR-tree is a chain of XOR gates each with one input pin connected to it which allows for pad to ball to trace connection testing.

The XOR testing methodology is to boot the part using straps to enter XOR mode (A description of the boot process follows). Once in XOR mode, all of the pins of an XOR chain are driven to logic 1. This action will force the output of that XOR chain to either a 1 if the number of the pins making up the chain is even or a 0 if the number of the pins making up the chain is odd.

Once a valid output is detected on the XOR chain output, a walking 0 pattern is moved from one end of the chain to the other. Every time the walking 0 is applied to a pin on the chain, the output will toggle. If the output does not toggle, there is a disconnect somewhere between die, package, and board and the system can be considered a failure.

12.1 XOR Test Mode Initialization

Figure 14. XOR Test Mode Initialization Cycles



The above figure shows the wave forms to be able to boot the part into XOR mode. The straps that need to be controlled during this boot process are BSEL[2:0], RSVD (Pin L18), EXP_SLR, and XORTEST.

On X48 Express Chipset platforms, all strap values must be driven before PWROK asserts. BSEL0 must be a "1". BSEL[2:1] need to be defined values, but logic value in any order will do. XORTEST must be driven to "0".

Not all of the pins will be used in all implementations. Due to the need to minimize test points and unnecessary routing, the XOR Chain 14 is dynamic depending on the values of EXP_SLR, and RSVD (Pin L18). See Figure 27 for what parts of XOR Chain 14 become valid XOR inputs depending on the use of EXP_SLR, and RSVD (Pin L18).

12.1.1 XOR Chain Definition

The MCH has 15 XOR chains. The XOR chain outputs are driven out on the following output pins. During full-width testing, XOR chain outputs will be visible on both pins.

Table 27. XOR Chain 14 Functionality

RSVD (Pin L18)	EXP_SLR	XOR Chain 14
1	0	EXP_RXP[15:0] EXP_RXN[15:0] EXP_TXP[15:0] EXP_TXN[15:0]
1	1	EXP_RXP[15:0] EXP_RXN[15:0] EXP_TXP[15:0] EXP_TXN[15:0]
0	0	EXP_RXP[15:8] EXP_RXN[15:8] EXP_TXP[15:8] EXP_TXN[15:8]
0	1	EXP_RXP[7:0] EXP_RXN[7:0] EXP_TXP[7:0] EXP_TXN[7:0]
1	0	EXP_RXP[15:0] EXP_RXN[15:0] EXP_TXP[15:0] EXP_TXN[15:0]
1	1	EXP_RXP[15:0] EXP_RXN[15:0] EXP_TXP[15:0] EXP_TXN[15:0]

Table 28. XOR Chain Outputs

XOR Chain	Output Pins	Coordinate Location
xor_out0	ALLZTEST	M21
xor_out1	XORTEST	L22
xor_out2	ICH_SYNCB	P16
xor_out3	RSVD	N18
xor_out4	RSVD	AN12
xor_out5	RSVD	AM14
xor_out6	BSEL1	F21
xor_out7	BSEL2	F18
xor_out8	RSVD	AN13
xor_out9	RSVD	AP12
xor_out10	EXP_SLR	K19
xor_out11	RSVD (Pin L18)	L18
xor_out12	BSEL0	M22
xor_out13	RSVD	H21
xor_out14	RSVD	G22

12.1.2 XOR Chains

This section provides the XOR chains.

Table 29. XOR Chain 0 (DDR3)

Pin Count	Ball #	Signal Name
	M21	ALLZTEST
1	B39	FSB_DB_56
2	D44	FSB_DB_52
3	B42	FSB_DB_55
4	D39	FSB_DB_57
5	C42	FSB_DB_51
6	C36	FSB_DB_58
7	A38	FSB_DB_49
8	B35	FSB_DB_62
9	D38	FSB_DB_54
10	E41	FSB_DB_50
11	D43	FSB_DB_53
12	D36	FSB_DB_59
13	E35	FSB_DB_63
14	E37	FSB_DB_61
15	F35	FSB_DB_48
16	C37	FSB_DB_60
17	F33	FSB_DB_26
18	B43	FSB_DB_18
19	F39	FSB_DB_17
20	F38	FSB_DB_16
21	H33	FSB_DB_25
22	G36	FSB_DB_22
23	G38	FSB_DB_20
24	G35	FSB_DB_23
25	L36	FSB_DB_19
26	L33	FSB_DB_29
27	L34	FSB_DB_27
28	N33	FSB_DB_28
29	N31	FSB_DB_30
30	K34	FSB_DB_24
31	M31	FSB_DB_31
32	K35	FSB_DB_21
33	L24	FSB_DB_44
34	H24	FSB_DB_45
35	G24	FSB_DB_47
36	K28	FSB_DB_40
37	K24	FSB_DB_46
38	F31	FSB_DB_32

Table 29. XOR Chain 0 (DDR3)

Pin Count	Ball #	Signal Name
39	L30	FSB_DB_36
40	G30	FSB_DB_38
41	N24	FSB_DB_42
42	H31	FSB_DB_34
43	H30	FSB_DB_39
44	L28	FSB_DB_41
45	M30	FSB_DB_35
46	N30	FSB_DB_37
47	K31	FSB_DB_33
48	L25	FSB_DB_43
49	E42	FSB_DB_15
50	F41	FSB_DB_14
51	G42	FSB_DB_11
52	G44	FSB_DB_13
53	H42	FSB_DB_9
54	J43	FSB_DB_8
55	H45	FSB_DB_12
56	L42	FSB_DB_7
57	M45	FSB_DB_5
58	M42	FSB_DB_3
59	L44	FSB_DB_6
60	J41	FSB_DB_10
61	P42	FSB_DB_0
62	N41	FSB_DB_1
63	N42	FSB_DB_4
64	N44	FSB_DB_2

Table 30. XOR Chain 1 (DDR3)

Pin Count	Ball #	Signal Name
	L22	XORTEST
1	H39	FSB_REQB_4
2	K42	FSB_AB_15
3	G40	FSB_REQB_1
4	K36	FSB_REQB_3
5	F43	FSB_AB_3
6	M36	FSB_AB_5
7	K38	FSB_AB_6
8	M38	FSB_AB_4

Table 30. XOR Chain 1 (DDR3)

Pin Count	Ball #	Signal Name
9	L40	FSB_AB_7
10	C44	FSB_REQB_0
11	M40	FSB_ADSTBB_0
12	N40	FSB_AB_9
13	L39	FSB_REQB_2
14	N36	FSB_AB_8
15	N39	FSB_AB_11
16	N38	FSB_AB_13
17	R35	FSB_AB_16
18	N34	FSB_AB_12
19	R39	FSB_AB_14
20	R36	FSB_AB_10
21	T34	FSB_AB_19
22	P43	FSB_AB_21
23	T40	FSB_AB_17
24	W34	FSB_AB_25
25	W36	FSB_AB_30
26	T38	FSB_AB_20
27	V35	FSB_AB_26
28	W33	FSB_AB_27
29	W38	FSB_AB_22
30	V34	FSB_ADSTBB_1
31	AA33	FSB_AB_31
32	T36	FSB_AB_18
33	AB35	FSB_AB_34
34	AA35	FSB_AB_32
35	V38	FSB_AB_23
36	AB34	FSB_AB_29
37	V39	FSB_AB_24
38	AA40	FSB_AB_33
39	V43	FSB_AB_28
40	AA38	FSB_AB_35

Table 31. XOR Chain 2 (DDR3)

Pin Count	Ball #	Signal Name
	P16	ICH_SYNCB
1	G34	FSB_DSTBNB_1
2	H34	FSB_DSTBPB_1
3	W41	FSB_RSB_1
4	R42	FSB_HITB
5	W40	FSB_TRDYB
6	V42	FSB_HITMB
7	M25	FSB_DSTBNB_2
8	N25	FSB_DSTBPB_2
9	K43	FSB_DSTBNB_0
10	J44	FSB_DSTBPB_0
11	T45	FSB_LOCKB
12	U42	FSB_BNRB
13	H38	FSB_BPRIB
14	D35	FSB_CPURSTB

Table 32. XOR Chain 3 (DDR3)

Pin Count	Ball #	Signal Name
	N18	RSVD
1	D41	FSB_DSTBNB_3
2	C40	FSB_DSTBPB_3
3	B37	FSB_DINVB_3
4	E40	FSB_DINVB_1
5	T39	FSB_DEFERB
6	R44	FSB_RSB_0
7	U41	FSB_DRDYB
8	T42	FSB_DBSYB
9	R41	FSB_RSB_2
10	N28	FSB_DINVB_2
11	L41	FSB_DINVB_0
12	W44	FSB_BREQ0B
13	U44	FSB_ADSB

Table 33. XOR Chain 4 (DDR3)

Pin Count	Ball #	Signal Name
	AN12	RSVD
1	AY41	DDR_A_ODT_1

Table 33. XOR Chain 4 (DDR3)

Pin Count	Ball #	Signal Name
2	BB39	DDR_A_CSB_1
3	BD42	DDR_A_CSB_0
4	BB44	DDR3_A_CSB1
5	BD37	DDR_A_MA_10
6	BB43	DDR_A_ODT_0
7	BD35	DDR3_A_MA0
8	BC36	DDR_A_MA_0
9	BA27	DDR_A_MA_9
10	BB30	DDR_A_MA_2
11	BB29	DDR_A_MA_3
12	BA29	DDR_A_MA_4
13	AV35	DDR_A_CKB_2
14	AT34	DDR_A_CK_2
15	AT33	DDR_A_CK_0
16	AN28	DDR_A_CK_1
17	AR33	DDR_A_CKB_0
18	AM28	DDR_A_CKB_1
19	BD29	DDR_A_MA_6
20	BB31	DDR_A_MA_1
21	BB28	DDR_A_MA_5
22	BC28	DDR_A_MA_8
23	AY27	DDR_A_MA_7
24	AY24	DDR_A_CKE_0
25	BB25	DDR_A_CKE_1
26	AV21	DDR_A_DQSB_3
27	AP21	DDR_A_DM_3
28	AY15	DDR_A_DQSB_2
29	BC14	DDR_A_DM_2
30	AY11	DDR_A_DQSB_1
31	BC10	DDR_A_DM_1
32	BC6	DDR_A_DQSB_0
33	BB5	DDR_A_DM_0

Table 34. XOR Chain 5 (DDR3)

Pin Count	Ball #	Signal Name
	AM14	RSVD
1	AA44	DDR_A_DQSB_7
2	AB40	DDR_A_DM_7
3	AD42	DDR_A_DQSB_6
4	AE44	DDR_A_DM_6
5	AM42	DDR_A_DQSB_5
6	AN44	DDR_A_DM_5
7	AT42	DDR_A_DQSB_4
8	AU44	DDR_A_DM_4
9	BA42	DDR_A_MA_13
10	BB41	DDR_A_CASB
11	BD39	DDR_A_WEB
12	BB36	DDR_A_BS_1
13	BC40	DDR3_A_WEB
14	BB38	DDR_A_RASB
15	BC37	DDR_A_BS_0
16	BA25	DDR_A_MA_14
17	BD27	DDR_A_MA_11
18	BB26	DDR_A_BS_2
19	BB27	DDR_A_MA_12
20	AK15	CL_DATA
21	AK14	CL_CLK

Table 35. XOR Chain 6 (DDR3)

Pin Count	Ball #	Signal Name
	F21	BSEL1
1	AA42	DDR_A_DQS_7
2	Y42	DDR_A_DQ_58
3	AA41	DDR_A_DQ_62
4	AB42	DDR_A_DQ_56
5	AB43	DDR_A_DQ_57
6	W42	DDR_A_DQ_59
7	AC40	DDR_A_DQ_60
8	Y45	DDR_A_DQ_63
9	AB39	DDR_A_DQ_61
10	AD43	DDR_A_DQS_6
11	AC42	DDR_A_DQ_50
12	AC39	DDR_A_DQ_55
13	AE41	DDR_A_DQ_48
14	AD40	DDR_A_DQ_54
15	AC45	DDR_A_DQ_51
16	AF42	DDR_A_DQ_52
17	AF45	DDR_A_DQ_53
18	AE42	DDR_A_DQ_49
19	AM43	DDR_A_DQS_5

Table 35. XOR Chain 6 (DDR3)

Pin Count	Ball #	Signal Name
20	AL40	DDR_A_DQ_46
21	AN41	DDR_A_DQ_40
22	AN42	DDR_A_DQ_41
23	AP42	DDR_A_DQ_44
24	AL41	DDR_A_DQ_47
25	AP45	DDR_A_DQ_45
26	AL42	DDR_A_DQ_43
27	AL44	DDR_A_DQ_42
28	AT43	DDR_A_DQS_4
29	AU43	DDR_A_DQ_33
30	AU41	DDR_A_DQ_37
31	AV42	DDR_A_DQ_32
32	AR41	DDR_A_DQ_38
33	AR40	DDR_A_DQ_39
34	AR44	DDR_A_DQ_34
35	AW42	DDR_A_DQ_36
36	AR42	DDR_A_DQ_35
37	AT21	DDR_A_DQS_3
38	AY21	DDR_A_DQ_25
39	AW19	DDR_A_DQ_29
40	AN21	DDR_A_DQ_30
41	AW22	DDR_A_DQ_31
42	AT22	DDR_A_DQ_27
43	AN22	DDR_A_DQ_26
44	AN19	DDR_A_DQ_24
45	AV19	DDR_A_DQ_28
46	BA15	DDR_A_DQS_2
47	BB16	DDR_A_DQ_18
48	BD15	DDR_A_DQ_22
49	BE16	DDR_A_DQ_19
50	BB14	DDR_A_DQ_17
51	BB15	DDR_A_DQ_23
52	BA13	DDR_A_DQ_20
53	BD13	DDR_A_DQ_16
54	BB13	DDR_A_DQ_21
55	BA11	DDR_A_DQS_1
56	BC9	DDR_A_DQ_13
57	BD11	DDR_A_DQ_14
58	BB11	DDR_A_DQ_15
59	BE12	DDR_A_DQ_11

Table 35. XOR Chain 6 (DDR3)

Pin Count	Ball #	Signal Name
60	BD9	DDR_A_DQ_8
61	BA9	DDR_A_DQ_12
62	BB12	DDR_A_DQ_10
63	BB10	DDR_A_DQ_9
64	BA6	DDR_A_DQS_0
65	BB7	DDR_A_DQ_7
66	BB8	DDR_A_DQ_2
67	BE8	DDR_A_DQ_3
68	BD7	DDR_A_DQ_6
69	BD4	DDR_A_DQ_1
70	BC4	DDR_A_DQ_0
71	BB4	DDR_A_DQ_5
72	BD3	DDR_A_DQ_4

Table 36. XOR Chain 7 (DDR3)

Pin Count	Ball #	Signal Name
	F18	BSEL2
1	AW44	DDR_A_ODT_3
2	AY43	DDR_A_CSB_3
3	BA41	DDR_A_ODT_2
4	BB39	DDR_A_CSB_2
5	AV31	DDR_A_CK_3
6	AT31	DDR_A_CKB_3
7	AT36	DDR_A_CKB_5
8	AT35	DDR_A_CK_5
9	AN27	DDR_A_CK_4
10	AM27	DDR_A_CKB_4
11	BC24	DDR_A_CKE_3
12	BB25	DDR_A_CKE_2
13	BB23	DDR3_DRAMRSTB

Table 37. XOR Chain 8 (DDR3)

Pin Count	Ball #	Signal Name
	AN13	RSVD
1	BB34	DDR_B_ODT_1

Table 37. XOR Chain 8 (DDR3)

Pin Count	Ball #	Signal Name
2	BD33	DDR_B_ODT_0
3	BB35	DDR_B_CSB_1
4	BA31	DDR_B_CSB_0
5	AV30	DDR_B_CKB_0
6	AW30	DDR_B_CK_0
7	AW33	DDR_B_CKB_2
8	AR28	DDR_B_CK_1
9	AP28	DDR_B_CKB_1
10	AV33	DDR_B_CK_2
11	BB21	DDR_B_MA_5
12	BB22	DDR_B_MA_2
13	BD21	DDR_B_MA_4
14	BC22	DDR_B_MA_1
15	AW24	DDR_B_MA_10
16	BB20	DDR_B_MA_6
17	BB19	DDR_B_MA_9
18	BE20	DDR_B_MA_8
19	BA21	DDR_B_MA_3
20	AY19	DDR_B_MA_7
21	BD17	DDR_B_CKE_0
22	AY22	DDR_B_MA_0
23	BD19	DDR_B_CKE_1
24	AR24	DDR_B_DQSB_3
25	AY25	DDR_B_DM_3
26	AP16	DDR_B_DQSB_2
27	AW16	DDR_B_DM_2
28	AR12	DDR_B_DQSB_1
29	AT13	DDR_B_DM_1
30	AT10	DDR_B_DQSB_0
31	AY8	DDR_B_DM_0

Table 38. XOR Chain 9 (DDR3)

Pin Count	Ball #	Signal Name
	AP12	RSVD
1	AD33	DDR_B_DQSB_7
2	AD35	DDR_B_DM_7
3	AG38	DDR_B_DQSB_6
4	AG35	DDR_B_DM_6

Table 38. XOR Chain 9 (DDR3)

Pin Count	Ball #	Signal Name
5	AP40	DDR_B_DQSB_5
6	AN36	DDR_B_DM_5
7	AV38	DDR_B_DQSB_4
8	AY40	DDR_B_DM_4
9	BA33	DDR_B_MA_13
10	BD31	DDR_B_RASB
11	BB32	DDR_B_CASB
12	AY31	DDR_B_WEB
13	AY18	DDR_B_MA_12
14	BA19	DDR_B_MA_11
15	BC18	DDR_B_MA_14
16	BB18	DDR_B_BS_2
17	BB24	DDR_B_BS_0
18	AW23	DDR_B_BS_1

Table 39. XOR Chain 10 (DDR3)

Pin Count	Ball #	Signal Name
	K19	EXP_SLR
1	AC33	DDR_B_DQS_7
2	AC36	DDR_B_DQ_62
3	AB32	DDR_B_DQ_58
4	AB38	DDR_B_DQ_59
5	AE34	DDR_B_DQ_61
6	AD36	DDR_B_DQ_57
7	AE35	DDR_B_DQ_60
8	AD39	DDR_B_DQ_56
9	AC34	DDR_B_DQ_63
10	AG39	DDR_B_DQS_6
11	AE38	DDR_B_DQ_51
12	AE33	DDR_B_DQ_55
13	AE39	DDR_B_DQ_50
14	AH33	DDR_B_DQ_52
15	AH34	DDR_B_DQ_48
16	AH36	DDR_B_DQ_53
17	AG33	DDR_B_DQ_49
18	AE40	DDR_B_DQ_54
19	AP39	DDR_B_DQS_5
20	AP35	DDR_B_DQ_42

Table 39. XOR Chain 10 (DDR3)

Pin Count	Ball #	Signal Name
21	AN39	DDR_B_DQ_46
22	AP36	DDR_B_DQ_41
23	AV36	DDR_B_DQ_44
24	AR34	DDR_B_DQ_45
25	AN40	DDR_B_DQ_47
26	AR36	DDR_B_DQ_40
27	AN33	DDR_B_DQ_43
28	AW39	DDR_B_DQS_4
29	AV39	DDR_B_DQ_38
30	AT40	DDR_B_DQ_35
31	AT38	DDR_B_DQ_34
32	AV40	DDR_B_DQ_39
33	AY39	DDR_B_DQ_32
34	AW38	DDR_B_DQ_33
35	AW36	DDR_B_DQ_37
36	AY38	DDR_B_DQ_36
37	AR25	DDR_B_DQS_3
38	AV27	DDR_B_DQ_27
39	AP27	DDR_B_DQ_31
40	AT25	DDR_B_DQ_30
41	AT27	DDR_B_DQ_26
42	AW25	DDR_B_DQ_24
43	AP24	DDR_B_DQ_29
44	AN24	DDR_B_DQ_28
45	AV25	DDR_B_DQ_25
46	AN18	DDR_B_DQS_2
47	AT19	DDR_B_DQ_19
48	AP19	DDR_B_DQ_18
49	AN16	DDR_B_DQ_20
50	AT18	DDR_B_DQ_22
51	AR18	DDR_B_DQ_23
52	AV16	DDR_B_DQ_17
53	AR16	DDR_B_DQ_21
54	AY16	DDR_B_DQ_16
55	AR13	DDR_B_DQS_1
56	AV15	DDR_B_DQ_11
57	AT15	DDR_B_DQ_10
58	AW13	DDR_B_DQ_13
59	AN15	DDR_B_DQ_14
60	AY13	DDR_B_DQ_9

Table 39. XOR Chain 10 (DDR3)

Pin Count	Ball #	Signal Name
61	AW12	DDR_B_DQ_12
62	AP15	DDR_B_DQ_15
63	AY12	DDR_B_DQ_8
64	AW10	DDR_B_DQS_0
65	AW8	DDR_B_DQ_0
66	AT11	DDR_B_DQ_2
67	AW11	DDR_B_DQ_7
68	AY7	DDR_B_DQ_1
69	AW6	DDR_B_DQ_5
70	AR11	DDR_B_DQ_6
71	AT12	DDR_B_DQ_3
72	AV8	DDR_B_DQ_4

Table 40. XOR Chain 11 (DDR3)

Pin Count	Ball #	Signal Name
	L18	RSVD
1	AY35	DDR_B_ODT_3
2	BA35	DDR_B_CSB_3
3	BB33	DDR_B_ODT_2
4	BA37	DDR3_B_ODT3
5	BC32	DDR_B_CSB_2
6	AY34	DDR_B_CKB_5
7	AW34	DDR_B_CK_5
8	AY28	DDR_B_CKB_4
9	AY30	DDR_B_CK_4
10	AP31	DDR_B_CKB_3
11	AR31	DDR_B_CK_3
12	BA17	DDR_B_CKE_3
13	BB17	DDR_B_CKE_2

Table 41. XOR Chain 12 (DDR3)

Pin Count	Ball #	Signal Name
	M22	BSEL0
1	V10	DMI_TXP_3
2	V11	DMI_TXN_3

Table 41. XOR Chain 12 (DDR3)

Pin Count	Ball #	Signal Name
3	V7	DMI_RXP_3
4	V6	DMI_RXN_3
5	R2	DMI_TXP_2
6	T1	DMI_TXN_2
7	P4	DMI_RXP_2
8	R5	DMI_RXN_2
9	N2	DMI_TXP_1
10	P3	DMI_TXN_1
11	T7	DMI_RXP_1
12	T8	DMI_RXN_1
13	R7	DMI_TXP_0
14	R6	DMI_TXN_0
15	N5	DMI_RXP_0
16	M4	DMI_RXN_0

Table 42. XOR Chain 13 (DDR3)

Pin Count	Ball #	Signal Name
	H21	RSVD
1	A8	PEG_TXN_7
2	B7	PEG_TXP_7
3	H10	PEG_RXN_7
4	G10	PEG_RXP_7
5	E9	PEG_TXN_6
6	D8	PEG_TXP_6
7	L12	PEG_RXN_6
8	K11	PEG_RXP_6
9	C10	PEG_TXN_5
10	B9	PEG_TXP_5
11	G12	PEG_RXN_5
12	H12	PEG_RXP_5
13	E11	PEG_TXN_4
14	D10	PEG_TXP_4
15	M13	PEG_RXN_4
16	N13	PEG_RXP_4
17	A12	PEG_TXN_3
18	B11	PEG_TXP_3
19	K13	PEG_RXN_3
20	L13	PEG_RXP_3

Table 42. XOR Chain 13 (DDR3)

Pin Count	Ball #	Signal Name
21	D12	PEG_TXN_2
22	E13	PEG_TXP_2
23	G13	PEG_RXN_2
24	H13	PEG_RXP_2
25	D14	PEG_TXN_1
26	E15	PEG_TXP_1
27	C14	PEG_RXN_1
28	B13	PEG_RXP_1
29	E17	PEG_TXN_0
30	D16	PEG_TXP_0
31	B15	PEG_RXN_0
32	A16	PEG_RXP_0
33	L2	PEG_TXN_15
34	M1	PEG_TXP_15
35	N10	PEG_RXN_15
36	N8	PEG_RXP_15
37	K4	PEG_TXN_14
38	L5	PEG_TXP_14
39	J2	PEG_RXN_14
40	K3	PEG_RXP_14
41	H4	PEG_TXN_13
42	J5	PEG_TXP_13
43	M8	PEG_RXN_13
44	M7	PEG_RXP_13
45	G2	PEG_TXN_12
46	H1	PEG_TXP_12
47	L10	PEG_RXN_12
48	M11	PEG_RXP_12
49	E4	PEG_TXN_11
50	F5	PEG_TXP_11
51	K8	PEG_RXN_11
52	K7	PEG_RXP_11
53	D3	PEG_TXN_10
54	F3	PEG_TXP_10
55	C2	PEG_RXN_10
56	D2	PEG_RXP_10
57	B4	PEG_TXN_9
58	B3	PEG_TXP_9
59	G6	PEG_RXN_9
60	F7	PEG_RXP_9

Table 42. XOR Chain 13 (DDR3)

Pin Count	Ball #	Signal Name
61	C4	PEG_TXN_8
62	C6	PEG_TXP_8
63	D5	PEG_RXN_8
64	E6	PEG_RXP_8

Table 43. XOR Chain 14 (DDR3)

Pin Count	Ball #	Signal Name
	G22	RSVD
1	AJ5	PEG2_TXN_7
2	AK4	PEG2_TXP_7
3	AE11	PEG2_RXN_7
4	AE10	PEG2_RXP_7
5	AH3	PEG2_TXN_6
6	AJ2	PEG2_TXP_6
7	AD12	PEG2_RXN_6
8	AE13	PEG2_RXP_6
9	AG5	PEG2_TXN_5
10	AH4	PEG2_TXP_5
11	AC7	PEG2_RXN_5
12	AC6	PEG2_RXP_5
13	AF1	PEG2_TXN_4
14	AG2	PEG2_TXP_4
15	AC10	PEG2_RXN_4
16	AC11	PEG2_RXP_4
17	AE5	PEG2_TXN_3
18	AF4	PEG2_TXP_3
19	AB12	PEG2_RXN_3
20	AC13	PEG2_RXP_3
21	AD3	PEG2_TXN_2
22	AE2	PEG2_TXP_2
23	AA7	PEG2_RXN_2
24	AA6	PEG2_RXP_2
25	AC4	PEG2_TXN_1
26	AD4	PEG2_TXP_1
27	AA11	PEG2_RXN_1
28	AA10	PEG2_RXP_1
29	AB1	PEG2_TXN_0

Table 43. XOR Chain 14 (DDR3)

Pin Count	Ball #	Signal Name
30	AB3	PEG2_TXP_0
31	AA13	PEG2_RXN_0
32	W12	PEG2_RXP_0
33	AP6	PEG2_TXN_15
34	AP7	PEG2_TXP_15
35	AP11	PEG2_RXN_15
36	AP10	PEG2_RXP_15
37	AT3	PEG2_TXN_14
38	AU2	PEG2_TXP_14
39	AL7	PEG2_RXN_14
40	AL6	PEG2_RXP_14
41	AR5	PEG2_TXN_13
42	AT4	PEG2_TXP_13
43	AL10	PEG2_RXN_13
44	AL11	PEG2_RXP_13
45	AP1	PEG2_TXN_12
46	AR2	PEG2_TXP_12
47	AK13	PEG2_RXN_12
48	AK12	PEG2_RXP_12
49	AN5	PEG2_TXN_11
50	AP4	PEG2_TXP_11
51	AH6	PEG2_RXN_11
52	AH7	PEG2_RXP_11
53	AM3	PEG2_TXN_10
54	AN2	PEG2_TXP_10
55	AH10	PEG2_RXN_10
56	AH11	PEG2_RXP_10
57	AL5	PEG2_TXN_9
58	AM4	PEG2_TXP_9
59	AH13	PEG2_RXN_9
60	AG12	PEG2_RXP_9
61	AK1	PEG2_TXN_8
62	AL2	PEG2_TXP_8
63	AE6	PEG2_RXN_8
64	AE7	PEG2_RXP_8

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